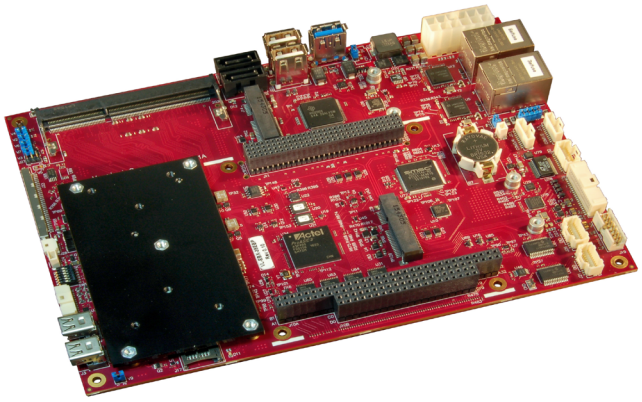

Hardware Reference Manual

REV. May 2018

Viper

(VL-EBX-38)

Intel® Atom™-based Single Board Computer with Dual Ethernet, Video, USB, SATA, Serial I/O, Digital I/O, Analog I/O, Trusted Platform Module security, Counter/Timers, Mini PCIe, mSATA, PC/104-*Plus* Interface, and SPX.

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Notice:

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Product Release Notes

Release 1.2	May 2018	Inserted an improved block diagram
Release 1.1	June 2017	Updated Power Delivery Considerations section
Release 1.0	March 2017	Initial Release

Technical Support

The EBX-38 support page, at EBX-38 Product Support Web Page, contains additional information and resources for this product including:

- Reference Manuals (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software
- VersaAPI .

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

If you have additional questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

RoHS Compliance

The EBX-38 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Cautions

Electrostatic Discharge

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EBX-38.

Lithium Battery

To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The Lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

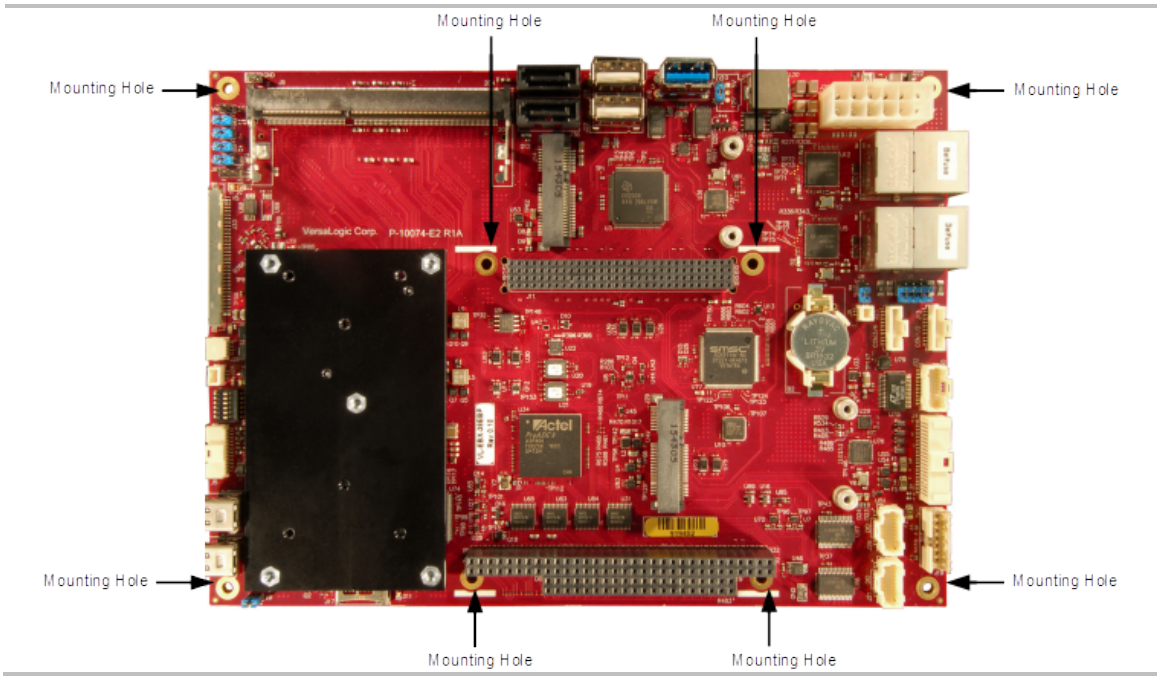
MOUNTING SUPPORT

The single board computer must be supported at all eight mounting points to prevent excessive flexing when expansion modules are attached and removed. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 5 for more details.

EARTH GROUND REQUIREMENT

All mounting standoffs should be connected to earth ground (chassis ground). This provides proper grounding for EMI purposes. The figure below shows the locations of the board's mounting holes. All mounting holes identified in below must be connected to earth ground.

Figure 1. Attaching the EBX-38 to Earth Ground



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Tables

1 Introduction

Description

The EBX-38 Viper is a low power / high-performance single board computer (SBC) which combines Intel's advanced Bay Trail processor, with a traditional PC/104-Plus* expansion interface. This combination makes it easy to upgrade existing systems to a powerful 4th generation Intel Atom* processor, while preserving plug-in expansion to existing specialty I/O boards. In addition, it also contains a full complement of on-board I/O interfaces, including USB 3.0, Mini PCIe expansion sockets, TPM chip, A/D, D/A, and 32-bits of digital I/O. Its features include:

- Intel Atom* "Bay Trail" processor, quad, dual, or single core with processor clock rates up to 1.91 GHz (Atom E38xx)
- Integrated Intel Gen 7 graphics core supports DirectX 11, OpenGL 4, and H.264, MPEG-2 encoding/decoding. Analog (VGA), Mini DisplayPort, and LVDS video outputs. DisplayPort supports HD audio output. Analog, dual channel LVDS, and Mini DisplayPort video outputs
- Up to 16 GB DDR3L memory per two SO-DIMM sockets for the quad and dual core processors, 8 GB DDR3L memory maximum with one SO-DIMM socket for the single core processor
- Two Intel I210-IT-based Ethernet ports, auto-detect 10Base-T / 100Base-TX / 1000Base-T
- One USB 3.0 port and six USB 2.0 ports
- Trusted Platform Module
- Four RS-232/422/485 serial ports
- Three 8254 timer/counters
- 8 general purpose I/Os
- 32 digital I/O lines
- 8 analog inputs
- 4 analog outputs
- 2 SATA ports, 3 Gb/s
- Mini PCIe / mSATA socket, supports Wi-Fi modems, GPS receivers, flash storage, and other modules
- Second Mini PCIe socket (without mSATA support)
- SPX expansion
- EBX form factor with PC/104-*Plus* expansion
- Customization available

The EBX-38 is compatible with popular operating systems such as Microsoft Windows*, Windows Embedded, Linux, VxWorks*, and QNX*.

EBX-38 boards are subjected to complete functional testing and are backed by a limited five-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional single-board computer (SBC).

The next figure shows the connectors and major components on the top side of the board.

Figure 3 shows the connectors and major components on the bottom side of the board.

Figure 2. VL-EBX-38 Viper Single Board Computer (Top Side)

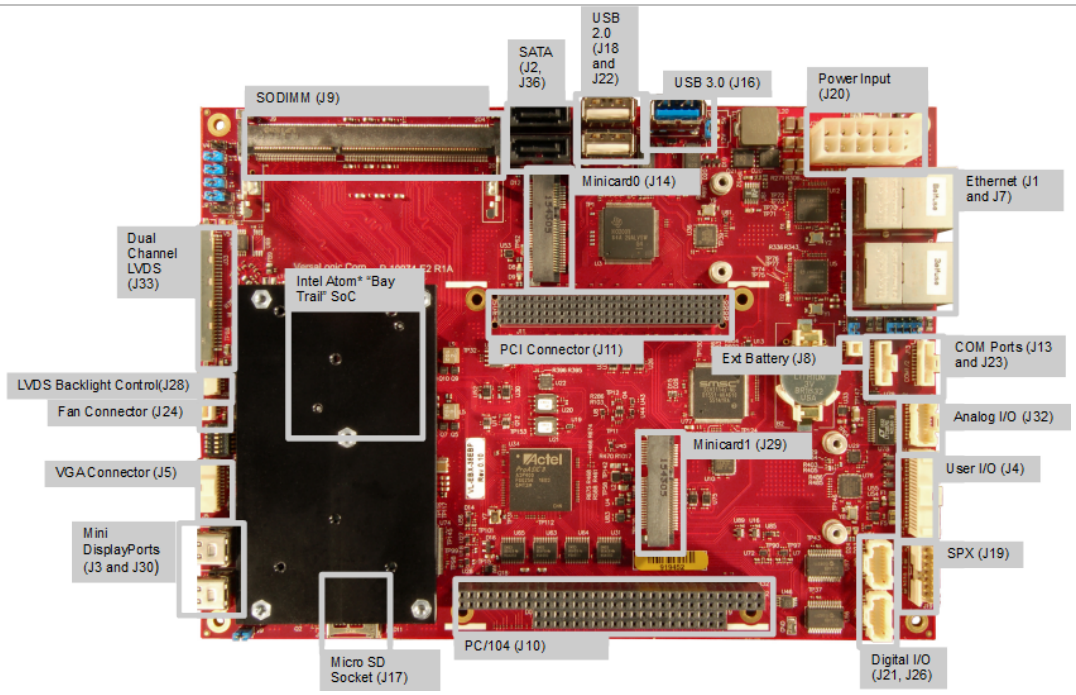
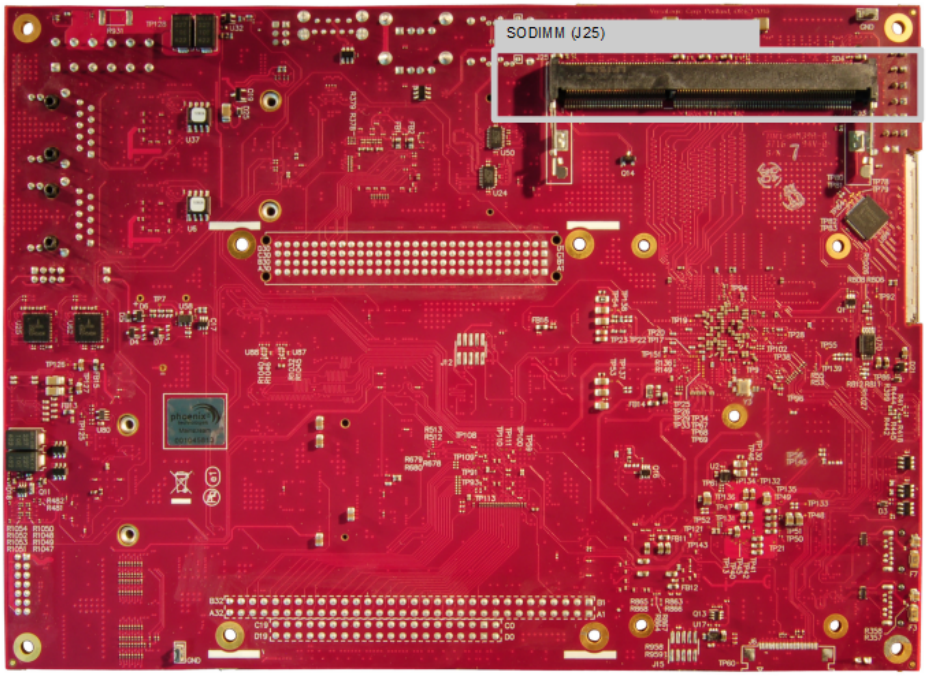


Figure 3. VL-EBX-38 Viper Single Board Computer (Bottom Side)



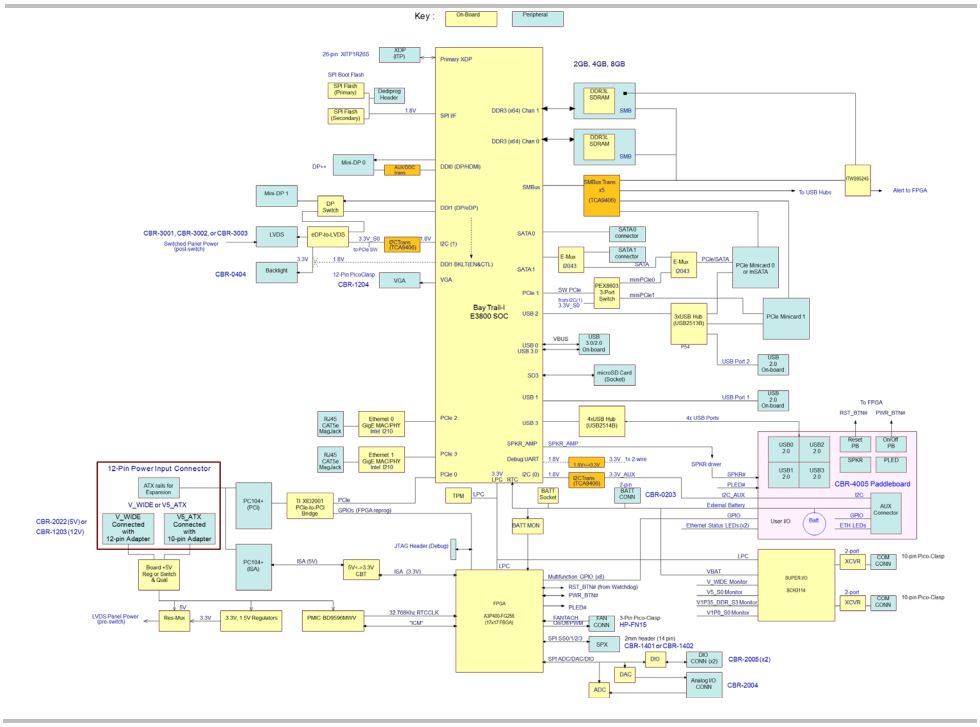
Technical Specifications

See the Viper Data Sheet for complete specifications.

Thermal Considerations

The operating temperature for the EBX-38 is -40 °C to +85 °C, de-rated -1.1 °C per 305m (1,000 ft.) above 2,300m (7,500 ft.). All Viper models include a rigid-mount heat plate thermal solution. Refer to the Chapter 13, beginning on page 60 for information on additional thermal solutions.

EBX-38 Block Diagram

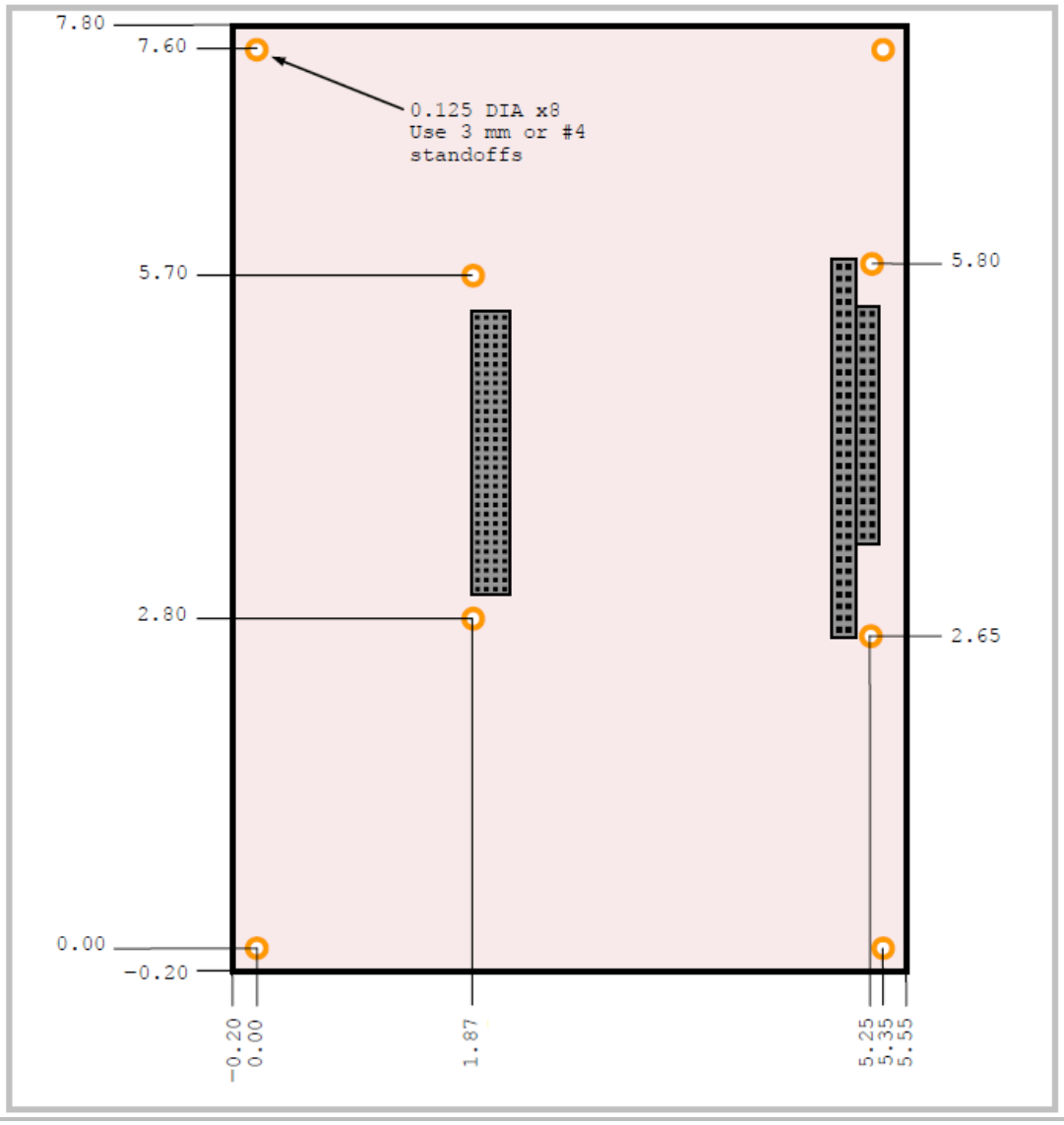


Dimensions and Mounting

The EBX-38 complies with the PC/104 standard which provides for specific mounting holes and PC/104-*Plus* stack locations as shown below.

Figure 4. EBX-38 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)



CAUTION:

The EBX-38 must be supported at all eight mounting points to prevent excessive flexing when expansion modules are attached and removed. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

HARDWARE ASSEMBLY

The EBX-38 mounts on four hardware standoffs using the corner mounting holes, and four more surrounding the PC/104-*Plus* area. These standoffs are secured to the underside of the circuit board using pan head screws for the corner mounts, and four more standoffs for the topside in PC/104-*Plus* area.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all standoffs to the mounting surface to prevent circuit board flexing.

An extractor tool is available (part number VL-HDW-203) to separate the PC/104 modules from the stack.

Related Documents

The following documents available are on the EBX-38 Product Support Web Page:

- *EBX-38 Programmer's Reference Manual* – provides information on the board's resources (memory, I/O, and IRQs), a description of the FPGA's registers, and programming information for the board's hardware interfaces.
- *VersaAPI Installation and Reference Guide* – describes the shared library of API calls for reading and controlling on-board devices on certain VersaLogic products.

Additional documents:

Processor Intel Atom E38xx (formerly "Bay Trail") System-on-Chip (SoC) Processor	Intel Atom Processor E3800 Product Family Datasheet
Ethernet Controller Intel I210-IT Gigabit Ethernet Controller	Intel I210-IT Datasheet
PC/104 Specification	http://www.versalogic.com/products/PC104/index.asp
PC/104-*Plus* Specification	http://www.versalogic.com/products/PC104/index.asp

Configuration and Setup 2

Initial Configuration

The following components are recommended for a typical development system.

- VL-EBX-38 single board computer
- VL-MM9-xxEBN DDR3L SO-DIMM module (see System RAM)
- ATX power supply with motherboard and disk drive connectors
- VGA video monitor
- USB Keyboard
- USB Mouse
- SATA hard drive

The following VersaLogic cables and accessories are recommended.

- EBX-38 cable kit (CKR-VIPER)
- VGA Video adapter cable (CBR-1204)
- User I/O cable (CBR-4005) and accompanying paddleboard (CBR-4005B)
- VL-CBR-0702 – SATA data cable
- VL-CBR-2022 – ATX to 5V power adapter (or VL-CBR-1203 ATX to 12V power adapter)
- (Cat5e cables)

Note: Only one of the listed power adapters can be used.

You will also need a Windows* (or other OS) installation CD/DVD and corresponding drive.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EBX-38 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EBX-38 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the Viper as well as their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

1. Install Memory

- Insert the DDR3L DRAM module into the SO-DIMM socket on the top side of the board and latch it into place. If you have an EBP or ECP SKU of the EBX-38, you may install a matching DDR3L DRAM module into the SO-DIMM socket on the bottom side of the board as well.

2. Attach Cables and Peripherals

- Plug the VGA cable VL-CBR-1204 into socket J5. Attach the cable to a VGA display. (Alternatively, you can attach a DisplayPort-enabled display to the Mini DisplayPort connectors at J3 or J30, or remove jumper V9 and connect J33 for LVDS panel (see jumper settings for LVDS resolutions).)
- Plug the VL-CBR-4005B paddleboard into socket J4.
- Plug a USB CD-ROM drive, USB keyboard, and USB mouse into any of the USB connectors of the CBR-4005B paddleboard.
- Plug the SATA data cable VL-CBR-0702 into socket J2 or J36. Attach a hard drive to the connector on the cable.
- Attach the SATA power adapter cable VL-CBR-0401 to the ATX power supply and SATA drive.
- Optionally, attach a LAN cable to either of the Ethernet connectors at J1 or J7 on the EBX-38.

3. Attach Power

- Plug the power adapter cable CBR-2022 into connector J20. Attach the motherboard connector of the ATX power supply to the adapter.
- Verify that the V10 jumper is selecting 5V (installed on pins 1 and 2).

4. Review Configuration

- Before you power up the system, double-check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EBX-38 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Select a Boot Drive

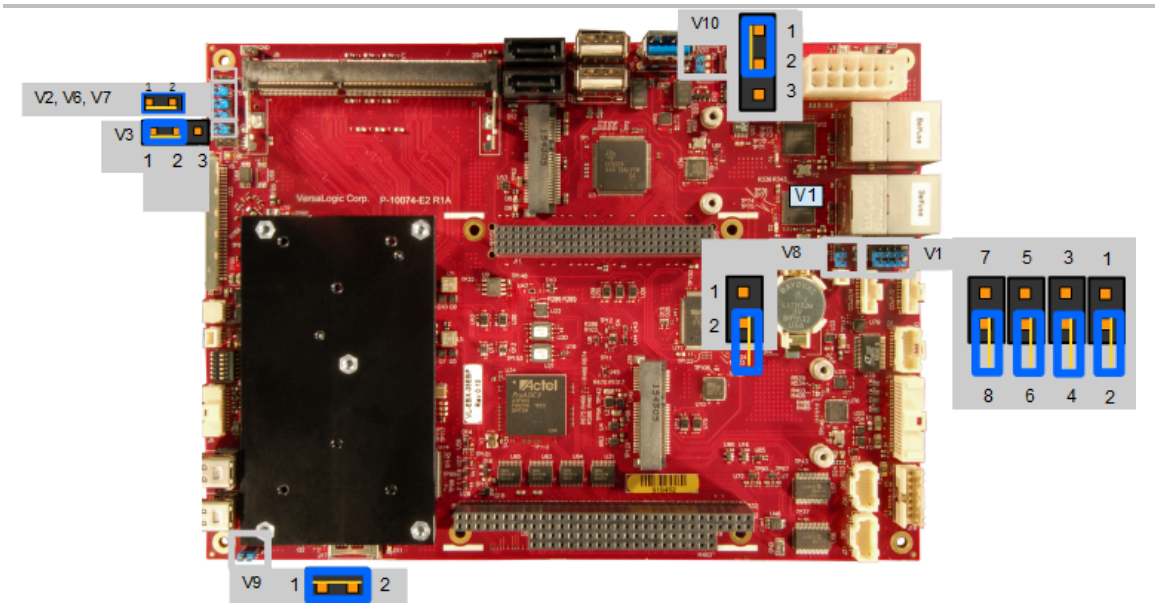
- During startup, press <CTRL> <B> to display the boot menu. Insert the OS installation CD in the CD-ROM drive and select to boot from the CD-ROM drive.

7. Install Operating System

- Install the operating system according to the instructions provided by the operating system manufacturer. (See Operating System Installation on page 13.)

Jumper Blocks

Figure 5. Jumpers Blocks in the As-Shipped Configuration



JUMPER SUMMARY

Table 1: V1 Jumper Summary

RS-422/485 120 Ohm Termination Jumper			
Jumper Pins	**Rx End-point Termination for**	**In**	**Out/Stored**
1 – 2	COM 1	RS-422 RS-485	RS-232 (Default)
3 – 4	COM 2	RS-422 RS-485	RS-232 (Default)
5 – 6	COM 3	RS-422 RS-485	RS-232 (Default)
7 – 8	COM 4	RS-422 RS-485	RS-232 (Default)

Table 2: V2 Jumper Summary

V2 Dual or Single Ended LVDS Mode	
Jumper Pins	**Description**
1 - 2	Single LVDS Mode when CFG1 = 0 (Default)
Store on pin 1	Dual LVDS Mode when CFG1 = 1

Table 3: V3 Jumper Summary

V3 Data Format and bpp	
Jumper Pins	**Description**
1 - 2	JEIDA or VESA 18 bpp when CFG2 = 1 (Default)
2 - 3	VESA 24 bpp when CFG2 = 0
Out (no jumper)	JEIDA 24 bpp when CFG2 floats

Table 4: V6, V7 Jumper Summary

V6. V7 (EDID Select – NXP PTN3460I Only)		
V6 **(CFG3)**	**V7** **(CFG4)**	**Function**
1-2 In (Low)	1-2 In (Low)	EDID #0
1-2 In (Low)	No Jumper (High)	EDID #1
No Jumper (High)	1-2 In (Low)	EDID #2
No Jumper (High)	No Jumper (High)	EDID #3

Table 5: V9 Jumper Summary

V9 DP1 Switch Output Selection Jumper	
Jumper Pins	**Description**
1 - 2	DP1 is passed to MiniDP1 J30 Connector FPGA_DP1_SW_SEL = 0
Store on pin 1	DP1 is passed to LVDS Bridge for LVDS output on J33 FPGA_DP1_SW_SEL = 1

Table 6: V10 Jumper Summary

V10 Power Input Selection Jumper	
Jumper Pins	**Description**
1 - 2	5V selection – enables V5_ATX switch
2 - 3	12V selection – enables V_WIDE voltage regulator
Removal of the jumpers disables both 5V_ATX and V_WIDE. The diodes ensure that there is always a voltage on the pullups on the jumpers. The pull resistors divide down V_WIDE by 1/3 to reduce the Vgs to less than 8V on the MOFSET. V5_ATX does not need to be divided down.	

Configuration Switches

The figure below shows the as-shipped switch configuration with all switches in the off position.

Figure 6. Location of SW1 Configuration Switch Block

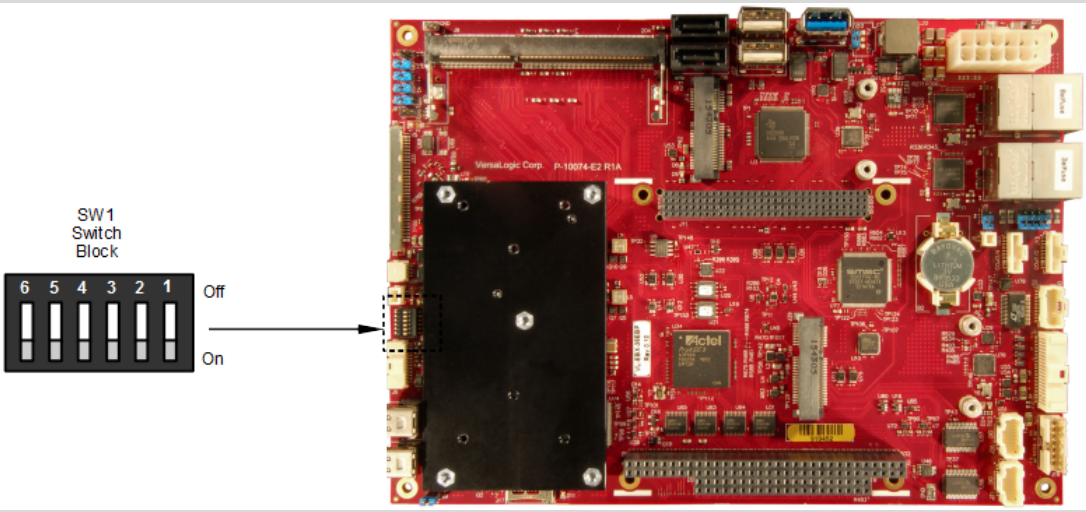


Table 7: Switch Setting Summary

SW1 Switch Position	Description
Position 1	**Clears non-volatile RAM and clears resets real-time clock registers (see page 12)** **Off** – Normal operation (default) On – Clears battery backed up non-volatile
Position 2	**No Battery Switch** (see Integrator's Note below) **Off** – A battery is being used (default) On – A battery is not being used

SW1 Switch Position	Description
Position 3	**Reset BIOS to factory defaults (see page 12)** **Off** – Normal operation (default) On – Resets BIOS to factory defaults when the board boots.
Position 4	**For factory use only. Always leave in the Off position.**
Position 5	**SPI Flash Security** – Not supported. Leave in the Off position.
Position 6	**BIOS select** **Off** – Primary BIOS (default) On – Backup BIOS

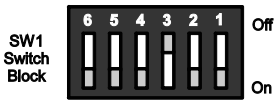
Integrator's Note:

- **If a battery is installed** (on the CBR-4005B paddleboard or externally using the J8 connector), switch position 2 must be set to the off position. If it is set to on, the battery will discharge quickly.
- **If you don't use a battery**, switch position 2 should be set to the on position. Otherwise, boot times could increase (by as much as 30 seconds in low temperature environments).

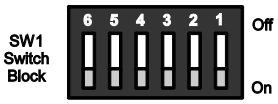
RESETTING THE BIOS TO FACTORY DEFAULTS

Reset the BIOS to default settings using the following the instructions:

1. Power off the EBX-38and set SW1 switch position 3 to the On position (toward the center of the board).



2. Power on the EBX-38.
3. After the system boots, power off the EBX-38 and set the switch back to the Off position (toward the outer edge of the board).

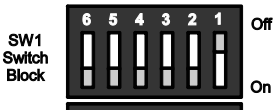


4. Power on the EBX-38.

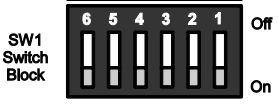
CLEARING RAM AND RTC REGISTERS

Clear RAM and RTC registers (which includes the date/time) using the following the instructions:

1. Power off the EBX-38.
2. Set SW1 switch position 1 to the On position (toward the center of the board).



3. Wait at least two seconds and set the switch back to the Off position (toward the outer edge of the board).



4. Power on the EBX-38.

BIOS Setup Utility

The EBX-38 permits users to modify the BIOS Setup utility defaults. Refer to the *EBX-38 BIOS Reference Manual* (available on the EBX-38 Product Support Web Page for information on accessing and configuring settings in the BIOS Setup utility. All BIOS menus, submenus, and configuration options are described in the *EBX-38 BIOS Reference Manual.*

Operating System Installation

The standard PC architecture used on the EBX-38 makes the installation and use of most of the standard x86 processor-based operating systems relatively simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EBX-38 Product Support Web Page

Board Features

3

CPU

The EBX-38 uses one of three Intel 4th Generation Atom (formerly "Bay Trail") System-on-Chip (SoC) processors:

- E3845 (quad core)
- E3826 (dual core)
- E3815 (single core)

Each core contains a 512 KB L2 cache. These processors support Intel 64-bit instructions, AES Instructions, Execute Disable Bit, and Virtualization Technology. See the Intel Atom Processor E3800 Product Family Datasheet for a complete description of the CPU.

Note: If the above link to the datasheet becomes inactive, search the internet for "Intel Bay Trail" or "E3800" and follow the results to the Intel site and datasheet.

System RAM

The EBX-38 accepts two SO-DIMM memory modules (J9 and J25) with the following characteristics:

- Size Up to 16 GB (8 GB per socket), 1066 MHz or 1333 MHz, CPU dependent
- Voltage 1.35 V
- Type DDR3L (VersaLogic VL-MM9 Series modules)

Note: Boards are designed for extended temperature use, so the memory refresh rate is always set to 3.9µs (double the standard refresh rate).
Single core processors can only utilize one SO-DIMM (J9).

I/O Interfaces

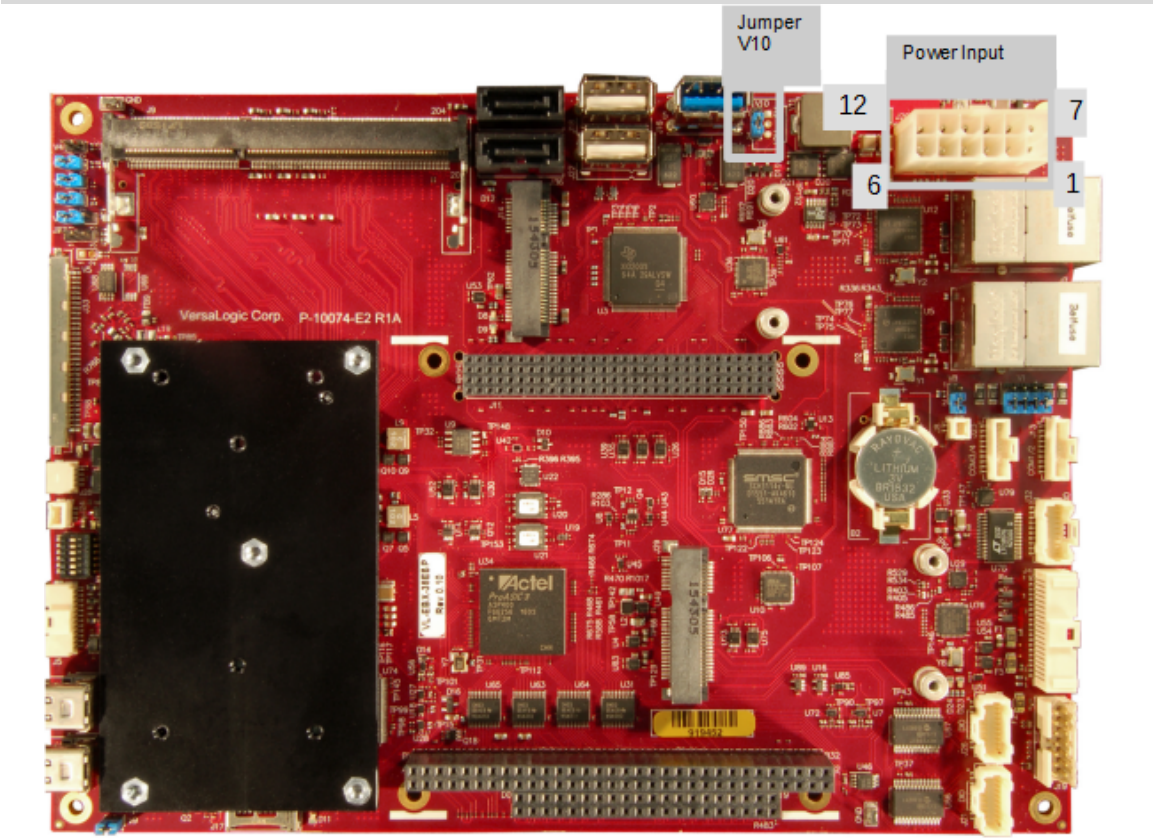
The EBX-38 board's I/O interfaces and their associated connectors are described in later chapters as follows:

Power Delivery

MAIN POWER CONNECTOR

The figure below shows the location and pin orientation of the main power connector.

Figure 7. Location and Pin Orientation of the Main Power Connector



CAUTION:

To prevent severe and possibly irreparable damage to the system, it is critical that the power connector is wired correctly. Make use of all +5 VDC pins and all ground pins to prevent excess voltage drop.

Note: The +3.3 VDC, +12 VDC and -12 VDC inputs on the power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require these voltages.

The table below lists the pinout for the main power connector.

Table 8: J20 Main Power Connector Pinout

Pin	Signal	Description
1	PS_ON#	Tied to Signal Ground on board (always enabled, active low)
2	GND	Signal Ground (see Note #1)
3	GND	Signal Ground (see Note #1)
4	+12V	Not used on-board but is passed through to PC/104 and PC/104-*Plus* connectors, board signal name is V12_ATX
5	+3.3V	Not used on-board but is passed through to PC/104-*Plus* +3.3V pins, board signal name is V3P3_ATX
6	+VIN	+9V to +15V (+12V Nominal) - board signal name is V_WIDE
7	+5VSTBY	Not connected - standby input power is not used
8	+5V	+5V - board signal name is V5_ATX
9	+5V	+5V - board signal name is V5_ATX
10	-12V	Not used on-board but is passed through to PC/104 and PC/104-*Plus*, board signal name is V12N_ATX
11	GND	Signal Ground (see Note #1)
12	+VIN	+9V to +15V (+12V Nominal) - board signal name is V_WIDE

Notes:

Note 1: Signal Ground must have low-impedance connection to Earth Ground somewhere in system for safety and EMI

Note 2: The max current per pin is 6 Amps. This limits the max +5V and +VIN power to 12 Amps. The 3 GND pins thus limits the total current to 18 Amps

Note 3: V10 jumper placement selects the voltage used for the board;V10[1:2] = 5V, V10[2:3] = 12V

Option 1 (Default)

Input Voltage	Power Connector	V10 Jumper Setting	Minimum Off Time for Power Cycling
+5V ±5%	V5_ATX (10-pin, 2 x 5)	Pin 1 to Pin 2	10 seconds

Option 2

Input Voltage	Power Connector	V10 Jumper Setting	Minimum Off Time for Power Cycling
+9V - +15V (+12V nominal)	V_WIDE (12-pin, 2 x 6)	Pin 2 to Pin 3	7 seconds

CABLING

An adapter cable, part number CBR-1203 (12V) or CBR-2022 (5V), is available for connecting the EBX-38 to an ATX power supply.

POWER DELIVERY CONSIDERATIONS

Using the VersaLogic approved 12V power supply (VL-PS-ATX12-300A) and power cable (VL-CBR-1203) or the 5V power supply (VL-PS200-ATX) and power cable (VL-CBR-2022) ensures high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

In addition, the specifications for typical operating current do not include any off-board power usage that may be fed through the main power connector. Expansion boards and USB devices plugged into the board will source additional power through the main power connector.

- Do not use wire smaller than 22 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18 inches.
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All power input pins and all ground pins must be independently connected between the power source and the power connector.
- Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

Refer to Table 24: PC/104-Plus Connectors Maximum Current on page 48 for information on the current ratings for the PC/104-*Plus* connectors.

POWER BUTTON

User I/O connector J4 includes an input for a push-button power switch. Shorting J4, pin 17 to ground causes the board to enter an S5 power state (similar to the Windows Shutdown state). Shorting it again returns the board to the S0 power state and reboots the board. The button can be configured in Windows to enter an S3 power state (Sleep, Standby, or Suspend-to-RAM), an S4 power state (Hibernate or Suspend-to-Disk), or an S5 power state (Shutdown or Soft-Off).

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 3.3 mA with a voltage drop that is less than 500 mV (there is a 1 kΩ resistor on the EBX-38 pulled up to 3.3 V). Do not add an external pull-up resistor to this signal.

A power button is provided on the CBR-4005B paddleboard. See Figure 24 on page 52 for the location of the power button on the CBR-4005B paddleboard.

In configurations where a power button is not connected to the board, if the system is put into an S5 state, power can be restored by turning off the power supply and turning it back on. This behavior is set by default in the BIOS.

SUPPORTED POWER STATES

This table lists the board's supported power states.

Table 9: Supported Power States

Power State	Description
S0 (G0)	Working
S1 (G1-S1)	All processor caches are flushed, and the CPUs stop executing instructions. Power to the CPUs and RAM is maintained. Devices that do not indicate they must remain on may be powered down.
S3 (G1-S3)	Commonly referred to as Standby, Sleep, or Suspend-to-RAM. RAM remains powered.
S4 (G1-S4)	Hibernation or Suspend-to-Disk. All content of main memory is saved to non-volatile memory, such as a hard drive, and is powered down.
S5 (G2)	Soft Off. Almost the same as G3 Mechanical Off, except that the power supply still provides power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can "wake" on input from the keyboard, clock, modem, LAN, or USB device.
G3	Mechanical off (ATX supply switch turned off).

BATTERY POWER OPTIONS

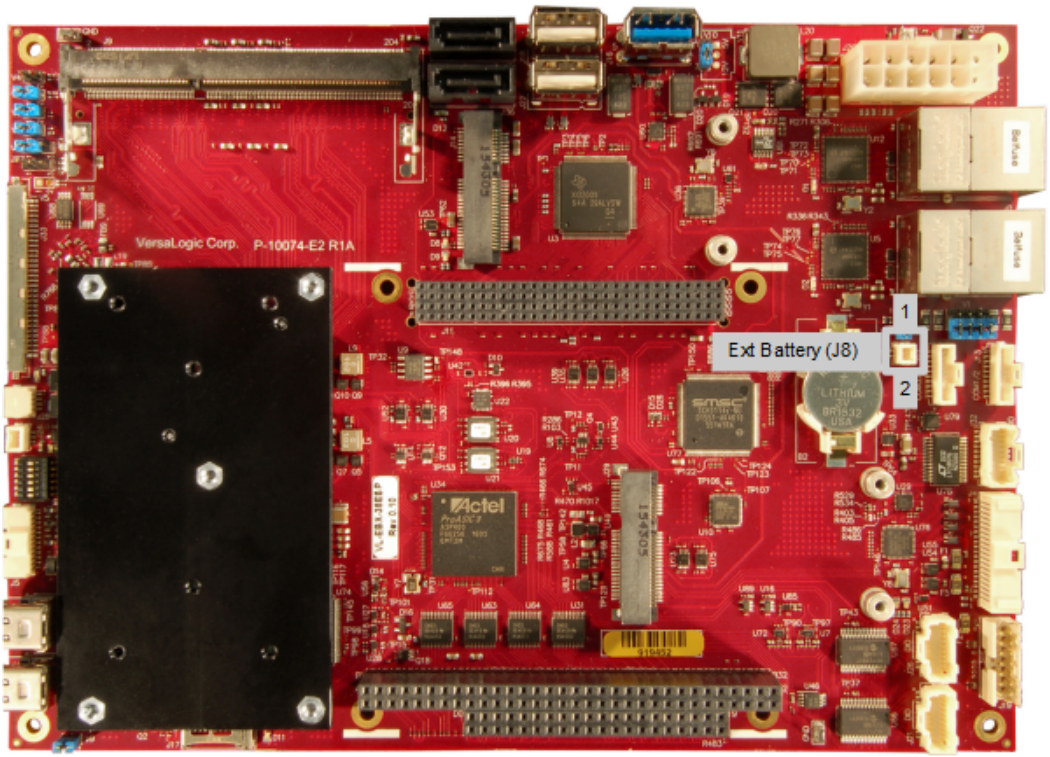
The battery circuit on the EBX-38 provides power for the Real-Time Clock (RTC) and power to store BIOS Setup utility settings in non-volatile RAM.

The EBX-38 has multiple options for providing battery power:

- Use an external battery, connected to the board through the J8 external battery connector.
- Use the battery supplied with the CBR-4005B paddleboard via the User I/O connector (J4).
- Use the on-board battery socket (B2).
- For custom designs only, a soldered in battery (B1 footprint is under B2) can replace the battery socket (B2) as the parts are dual-footprinted.

The figure below shows the location and pin orientation of the external battery connector.

Figure 8. Location and Pin Orientation of the External Battery Connector



CABLING

If your application requires a custom cable, the following information will be useful:

EBX-38 Board Connector	Mating Connector
Molex 501331-0207	Molex 501330-0200

VL-CBR-0203 External Battery Module

The VL-CBR-0203 external battery module is compatible with the EBX-38. For more information, contact Sales@VersaLogic.com.

Figure 9. VL-CBR-0203 Latching Battery Module

Real Time Clock (RTC)

The EBX-38 features a real-time clock/calendar (RTC) circuit. The RTC can be set using the BIOS Setup utility.

The EBX-38 supplies RTC voltage in S4, S3, and S0 states, but requires an external +2.75 V to +3.3 V battery to maintain RTC functionality and RTC CMOS RAM when the board is not powered. The battery connection can be made to any and all of the following:

- B2 on-board battery socket per the V8 jumper placed on pins 1-2
- J8 external battery connector
- J4 user I/O connector

Push-Button Reset

User I/O connector J4 includes an input for a push-button reset switch. Shorting J4, pin 18 to ground causes the EBX-38 to reboot.

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 3.3 mA with a voltage drop that is less than 500 mV (there is a 1 kΩ resistor on the EBX-38 pulled up to 3.3 V). Do not add an external pull-up resistor to this signal.

Integrator's Note:

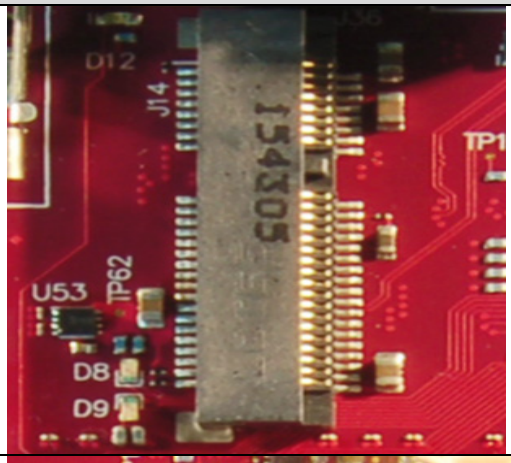
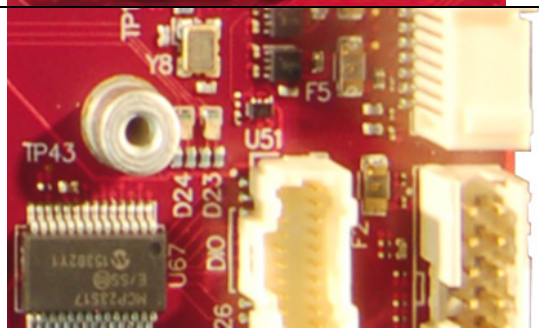
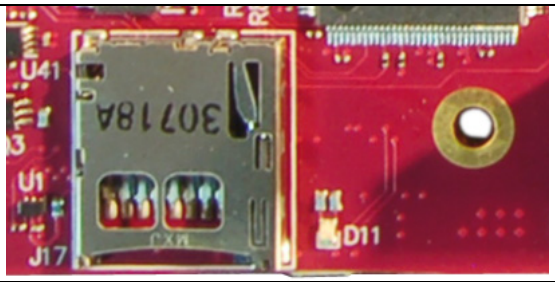
The reset button has a switch de-bounce circuit in the FPGA that requires the button to be held asserted at least 125 ms (1/8 second) to reset the board. Holding the reset asserted on a Bay Trail processor does not continue to hold the processor in reset; it only resets on the edge of the assertion that follows the 125 ms de-bounce time interval).

A reset button is provided on the CBR-4005B paddleboard. See Figure 24 on page 52 for the location of the reset button on the CBR-4005B paddleboard.

LEDs/Indicators

This table shows the locations of the boards LEDs/indicators.

Figure 10. Locations of the LEDs/Indicators

LED	Description	Location
D8/D9	PCIe Mini Card 0 LEDs	
D23/D24	PCIe Mini Card 1 LEDs	
D11	FPGA Debug LED GRN: On = S0 power is good, blinks when in S3 sleep state. YEL: On with warning or error.	
D12	SATA Activity LED	Near SATA connectors
D22	Panel Power Status LED	Near LVDS connector J33
J1	Integrated RJ45 Ethernet 0 LEDs	 Left is green (link/activity), Right is yellow (1Gbit Speed) indicator.

LED	Description	Location
J7	Integrated RJ45 Ethernet 1 LEDs	 Left is green (link/activity), Right is yellow (1Gbit Speed) indicator.

PROGRAMMABLE LED

User I/O connector J4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J4, pin 16; connect the anode to +3.3 V. An on-board 120 Ω resistor limits the current when the circuit is turned on. A programmable LED is provided on the CBR-4005B paddleboard. See Figure 24 on page 52 for the location of the Programmable LED on the CBR-4005B paddleboard.

For instructions on how to switch the Programmable LED on and off, refer to the *EBX-38 Programmer's Reference Manual* (available on the EBX-38 Product Support Web Page)

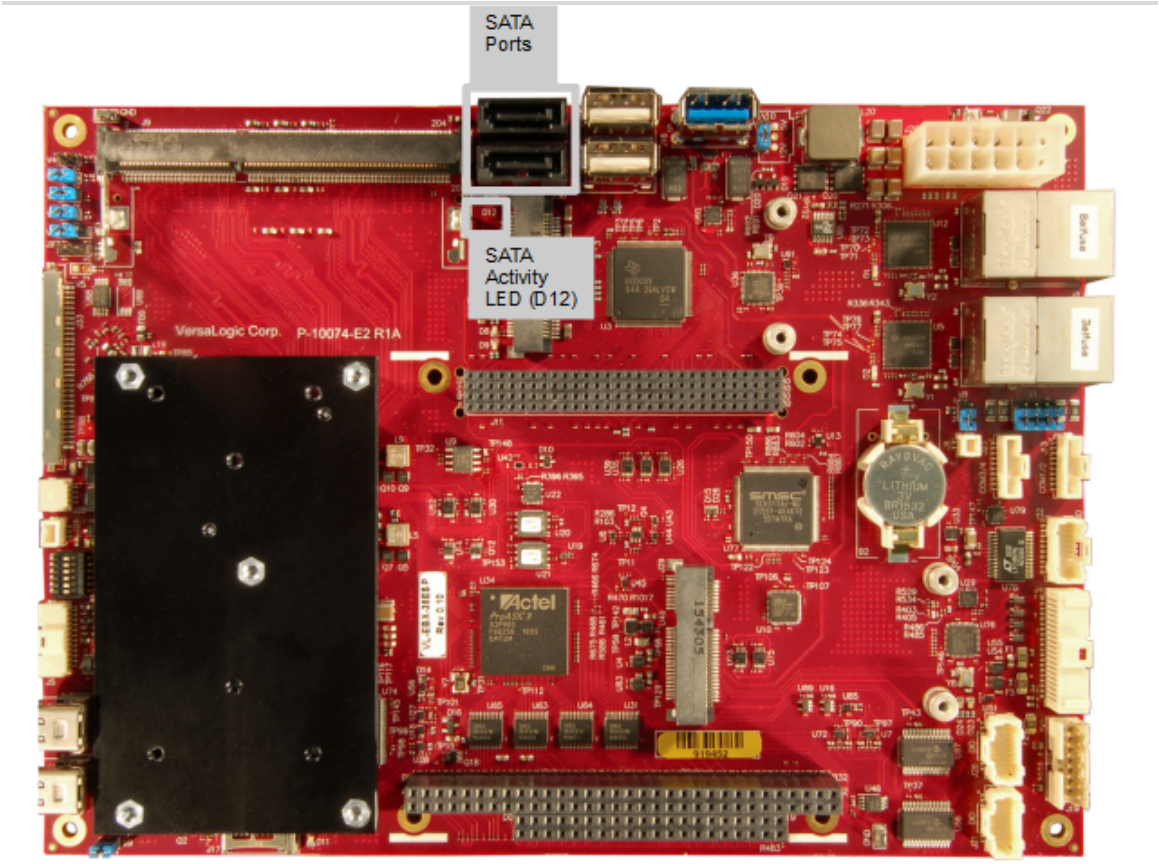
External Speaker

A miniature 8 Ω speaker can be connected between user I/O connector J4, pin 15 (SPKR#) and J4, pin 13 (V3P3). A speaker is provided on the CBR-4005B paddleboard. See CBR-4005B Paddleboard on page 51 for the location of the speaker on the CBR-4005B paddleboard.

SATA

The EBX-38 provides two SATA 2.0 ports (J2 and J36). When mSATA is used, the SATA channel for J36 will not be available. Power to the SATA drive is provided by the ATX power supply. Note that the standard SATA drive power connector is different from the typical 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

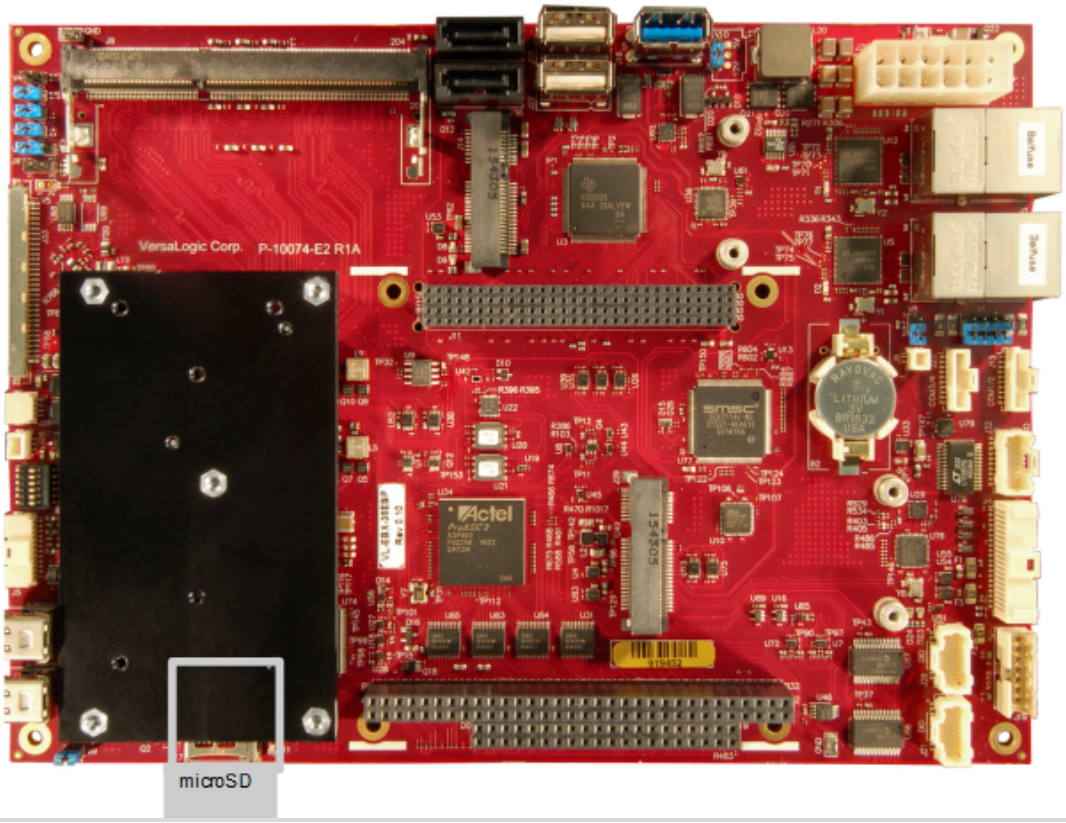
Figure 11. Location of the SATA Ports



microSD Socket

The figure below shows the location of the microSD socket. The VL-F41 series of microSD cards provide solid-state storage of 2 GB, 4 GB, or 8 GB. The microSD socket accommodates cards with up to 64 GB of storage capacity. No drivers are needed, as the device interface is abstracted as a standard parallel IDE drive on the master IDE channel.

Figure 12. Location of the microSD Socket



USB Interfaces

The EBX-38 offers a total of 1 on-board USB 3.0 port, 4 off-board (paddleboard) USB 2.0 ports, and 4 on-board USB ports (2 to the Type A connectors and two for the Mini Cards). An additional USB 2.0 port is paired with the USB 3.0 port. This configuration requires two USB hubs; one USB2513B and one USB2514B as shown in the EBX-38 Block Diagram. The figure below shows the location of the USB ports on the baseboard.

This interface can operate using either the Atom processor's EHCI controller or its xHCI controller. To use the USB 3.0 Super Speed mode, the xHCI controller must be used. USB controller selection is set in the BIOS. By default, EHCI is used. Some older operating systems (such as MS-DOS) may not support xHCI.

Figure 13. Location of the USB Ports

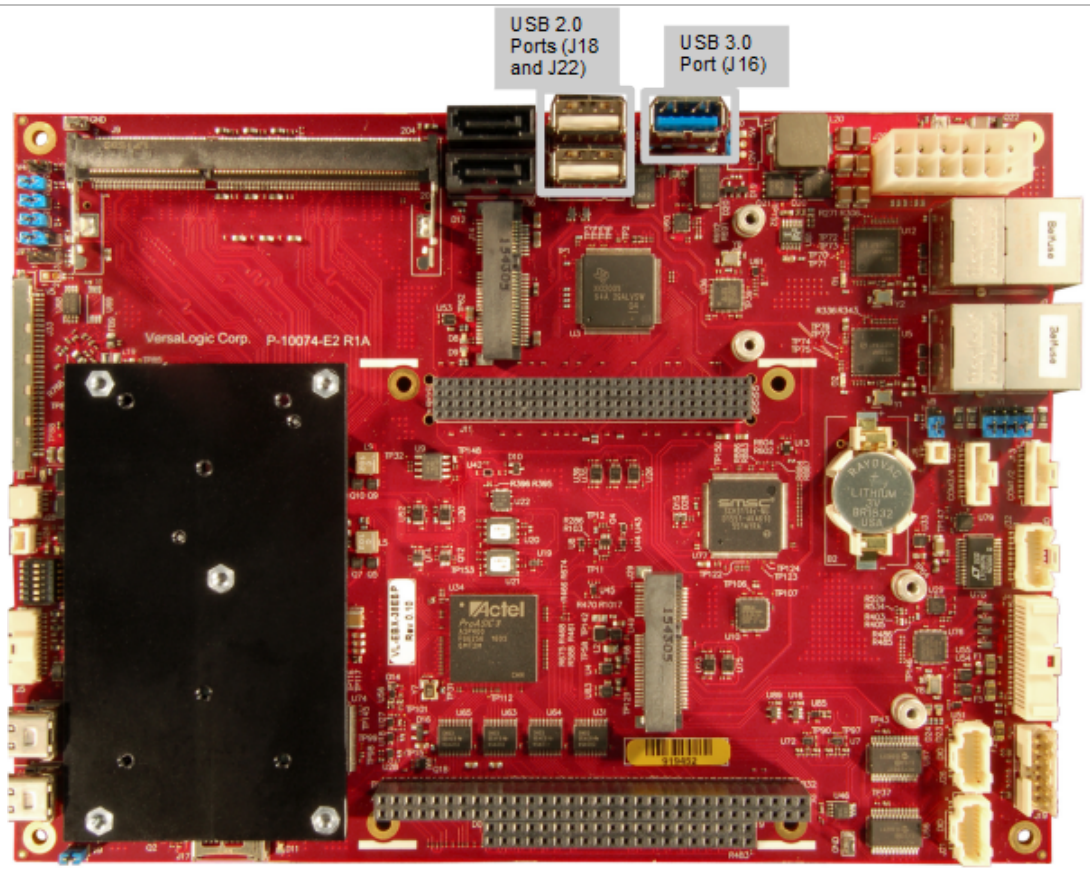


Table 10: USB 3.0 J16 Connector Pinout

J16 Pin	Signal Name	Direction	Function
1	+5V	Out	VBUS Voltage (max 900mA)
2	USB-	I/O	USB 2.0 Diff pair negative
3	USB+	I/O	USB 2.0 Diff pair positive
4	Signal Ground	--	
5	StdA_SSRX-	In	USB 3.0 Negative Rx Diff Pair
6	StdA_SSRX+	In	USB 3.0 Positive Rx Diff Pair
7	Signal Ground	--	
8	StdA_SSTX-	Out	USB 3.0 Negative Tx Diff Pair
9	StdA_SSTX+	Out	USB 3.0 Positive Tx Diff Pair

Note: Shield is Earth-Grounded (4 board holes but only have to Earth-GND one - shield ties them together).

PCIe Mini Card / mSATA

The sockets in J14 and J29 accept full-height PCI Express Mini Cards or mSATA modules. The mSATA interface is supported on J14 only. Additionally only two SATA channels are supported at one time, either J2 and J36 (both SATA connectors), or J2 (SATA connector) and J14 (mSATA).

The PCIe Mini Card interface includes one PCIe x1 lane, one hubbed USB 2.0 channel, and the SMBus interface. The socket is compatible with plug-in Wi-Fi modems, GPS receivers, Flash data storage, and other cards for added flexibility. The VL-MPEs-F1E series of mSATA modules provide flash storage of 4 GB, 16 GB, or 32 GB.

For more information on PCIe Mini Cards offered by VersaLogic, contact Sales@VersaLogic.com.

To secure a Mini Card or mSATA module to the on-board standoffs, use two M2.5 x 6mm pan head Philips nylon screws. These screws are available in quantities of 10 in the VL-HDW-108 hardware kit from VersaLogic.

Table 11: PCIe Mini Card / mSATA Pinout

J14 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
1	WAKE#	Wake	Reserved	Not connected
2	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
3	NC	Not connected	Reserved	Not connected
4	GND	Ground	GND	Ground
5	NC	Not connected	Reserved	Not connected
6	1.5V	1.5V power	+1.5V	1.5V power
7	NC	Not connected	Reserved	Not connected
8	NC	Not connected	Reserved	Not connected
9	GND	Ground	GND	Ground
10	NC	Not connected	Reserved	Not connected
11	REFCLK-	Reference clock input –	Reserved	Not connected
12	NC	Not connected	Reserved	Not connected
13	REFCLK+	Reference clock input +	Reserved	Not connected

J14 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
14	NC	Not connected	Reserved	Not connected
15	GND	Ground	GND	Ground
16	NC	Not connected	Reserved	Not connected
17	NC	Not connected	Reserved	Not connected
18	GND	Ground	GND	Ground
19	NC	Not connected	Reserved	Not connected
20	W_DISABLE#	Wireless disable	Reserved	Not connected
21	GND	Ground	GND	Ground
22	PERST#	Card reset	Reserved	Not connected
23	PERn0	PCIe receive –	+B	Host receiver diff. pair +
24	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
25	PERp0	PCIe receive +	-B	Host receiver diff. pair –
26	GND	Ground	GND	Ground
27	GND	Ground	GND	Ground
28	1.5V	1.5V power	+1.5V	1.5V power
29	GND	Ground	GND	Ground
30	SMB_CLK	SMBus clock	Two Wire I/F	Two wire I/F clock
31	PETn0	PCIe transmit –	-A	Host transmitter diff. pair –
32	SMB_DATA	SMBus data	Two Wire I/F	Two wire I/F data
33	PETp0	PCIe transmit +	+A	Host transmitter diff. pair +
34	GND	Ground	GND	Ground
35	GND	Ground	GND	Ground
36	USB_D-	USB data –	Reserved	Not connected
37	GND	Ground	GND	Ground
38	USB_D+	USB data +	Reserved	Not connected
39	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
40	GND	Ground	GND	Ground
41	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
42	LED_WWAN#	Wireless WAN LED	Reserved	Not connected
43	GND	GND	GND/NC	GND)
44	LED_WLAN#	Wireless LAN LED	Reserved	Not connected
45	NC	Not connected	Vendor	Not connected
46	LED_WPAN#	Wireless PAN LED	Reserved	Not connected
47	NC	Not connected	Vendor	Not connected
48	1.5V	1.5V power	+1.5V	1.5V power
49	Reserved	Reserved	DA/DSS	Device activity (**Note 1**)
50	GND	Ground	GND	Ground
51	PRES_DISABLE 2#	PCIe Mini Card vs. mSATA detection	GND	Ground (**Note 2)**
52	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source

Notes:

1. This signal is not currently implemented in the FPGA to drive the blue LED activity indicator.
2. Some PCIe modules use this signal as a second Mini Card wireless disable input. On the Viper, this signal is available for use for mSATA versus PCIe Mini Card detection. There is an option in BIOS setup for setting the mSATA detection method.

PCIe Mini Card LEDs

The Mini Card specification states that there are three LED outputs: WWAN, WLAN and WPAN. There are on-board LEDs for each of these. A fourth LED is used to indicate when the Mini Card is powered (since the Mini Card power can be configured to either be always-on or on in S0). This indicator is very important as a warning to NOT hot-plug the Mini Card (otherwise it might appear it is OK when the board is in a sleep mode but the Mini Card is still powered); as a result, it is intentionally yellow to indicate "caution".

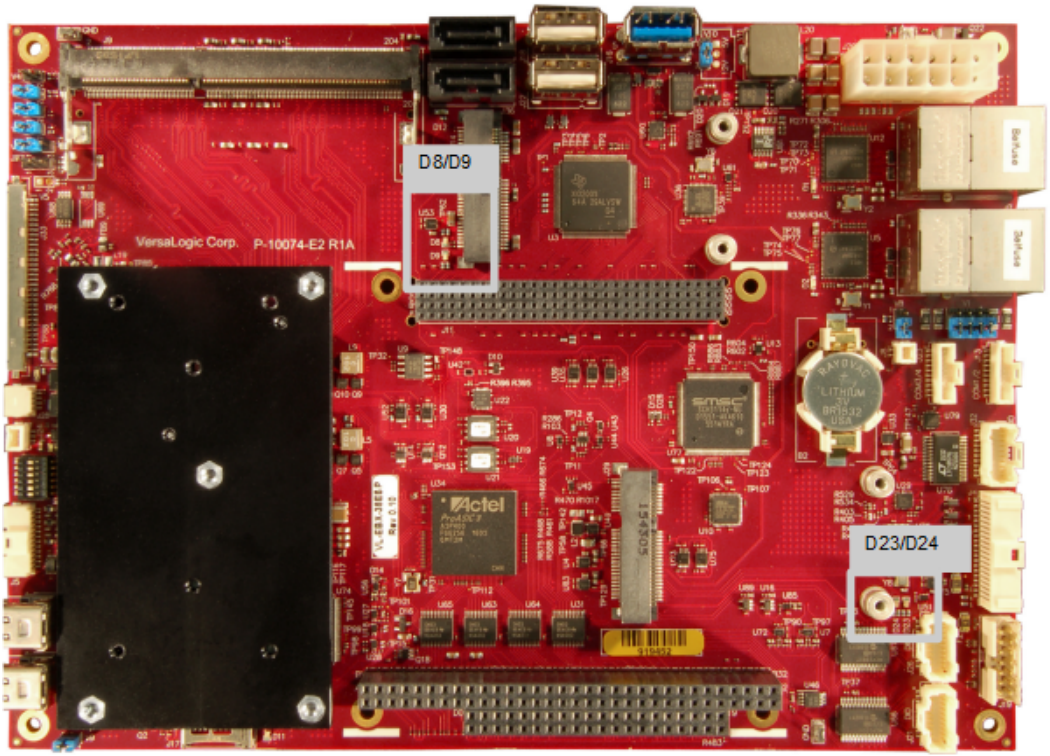
Table 12: PCIe Mini Card LED States

LED	Ref Des	State	Description
Green (WWAN)	D8 (Mini0)	On	WWAN active
	D23 (Mini1)	Off	WWAN inactive
Yellow (WLAN)	D8 (Mini0)	On	WLAN active
	D23 (Mini1)	Off	WLAN inactive
Green (WPAN)	D9 (Mini0)	On	WPAN active
	D24 (Mini1)	Off	WPAN inactive
Yellow (Power On)	D9 (Mini0)	On	Mini Card Power is On
	D24 (Mini1)	Off	Mini Card Power is Off

Integrator's Note:

The 3.3 V power to the Mini Card can be controlled by the FPGA. By default, the power is always on, but there is a register setting that turns this power off in sleep modes. The Mini Card 1.5 V power is always turned off in sleep modes.

Figure 14. Location of PCIe Mini Card LEDs



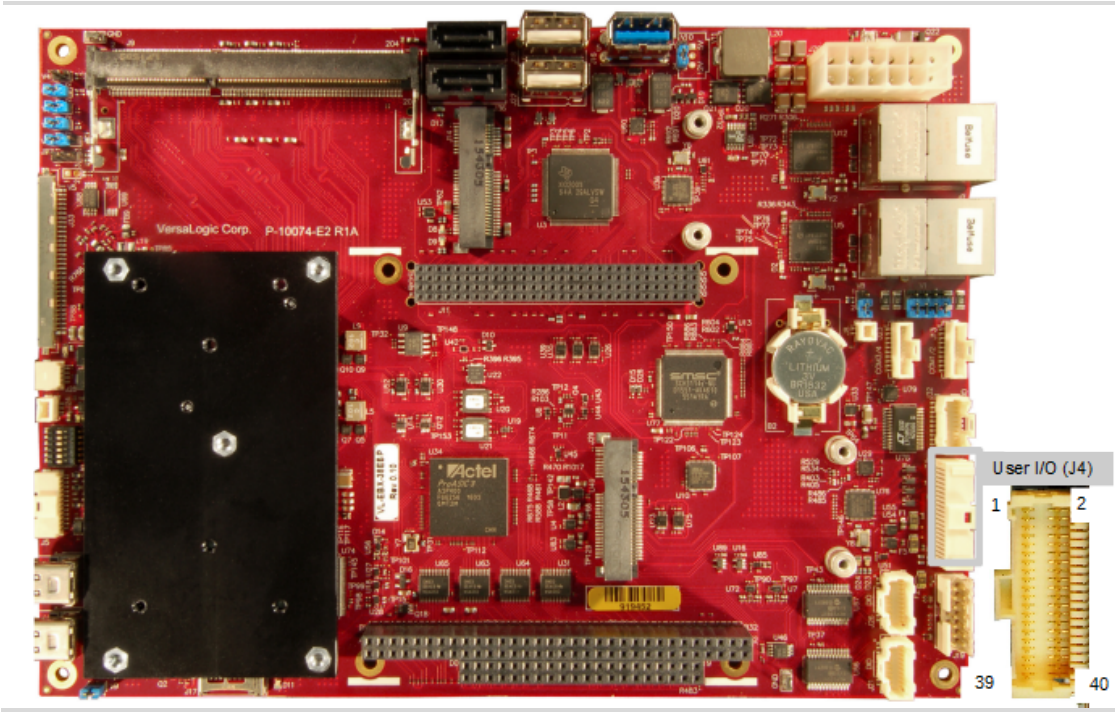
User I/O Connector

The 40-pin J4 I/O connector incorporates the signals for the following:

- Four USB ports
- Eight GPIO lines (these are functionally muxed with six timer I/O signals per FPGA registers). The eight GPIO lines on the paddleboard each have an alternate mode, accessible using the FPGA's AUXMOD1 register. Refer to the *EBX-38 Programmer's Reference Manual* for more information on FPGA registers.
- Three LEDs (two Ethernet link status LEDs and a programmable LED)
- Push-button power switch
- Push-button reset switch
- Speaker output

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage. The figure below shows the location and pin orientation of the user I/O connector.

Figure 15. Location and Pin Orientation of User I/O Connector



This table provides the pinout of the user I/O connector.

Table 13: J4 I/O Connector Pinout and Pin Orientation

Pin	Signal	Pin	Signal
1	+5 V (V5_USB01)	2	GND
3	USB0_P	4	USB1_P
5	USB0_N	6	USB1_N
7	+5V (V5_USB23)	8	GND
9	USB2_P	10	USB3_P
11	USB2_N	12	USB3_N
13	+3.3 V (**Note 1**)	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	Reserved	22	V_BATT
23	Reserved	24	RETURN_BATT
25	GND	26	GND
27	FPGA GPIO1	28	FPGA GPIO2
29	FPGA GPIO3	30	FPGA GPIO4
31	GND	32	GND
33	FPGA GPIO5	34	FPGA GPIO6
35	FPGA GPIO7	36	FPGA GPIO8
37	+3.3 V (**Note 2**)	38	GND
39	ETH0 LED	40	ETH1 LED

Notes:

1. This 3.3 V power goes off in sleep modes. The SPKR# uses this power as should the PLED# (there is no requirement for PLED# to use this power, but the CBR-4005 paddleboard does).

2. This 3.3 V power can be turned on or off similar to the 3.3V power to the Mini Card via the FPGA (can go off in sleep modes or always stay on; by default it goes off in sleep modes). It is used for the 10 kΩ pullup resistor power on the 8x GPIOs and usually for the 2x Ethernet LEDs, however, the Ethernet LEDs can be powered by a 3.3 V power source.

CABLING

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EBX-38. This is a 12-inch, Pico-Clasp 40-pin to 40-pin cable

If your application requires a custom cable, the following information will be useful:

EBX-38 Board Connector	Mating Connector
Molex 501571-4007	Molex 501189-4010

Digital I/O (DIO)

The 20-pin I/O connectors (J21 and J26) incorporate 16 (per connector) Digital I/O (DIO) lines that are independently configurable as input or output. DIO inputs can be set for normal or inverted level. DIO outputs can be set to be normal HIGH or LOW state. Any I/O pin can also be configured to generate an interrupt on a change of state. There are pull-up resistors to +3.3 V on all DIO lines. The pull-ups implemented on-board are 10kΩ values. After reset, the DIO lines are set as inputs with pull-ups that will be detected as a HIGH state to external equipment.

VersaLogic provides a set of application programming interface (API) calls for managing the DIO lines. See the VersaAPI Support Page for information.

The figure below shows the location of the digital I/O connectors. Table 14 lists the pin functions of the digital I/O connectors and how the pins are routed via the VL-CBR-2005A to the VL-CBR-2004B paddleboard. Refer to page 56 for information on the VL-CBR-2004B paddleboard.

Figure 16. Location and Pin Orientation of Digital I/O Connector

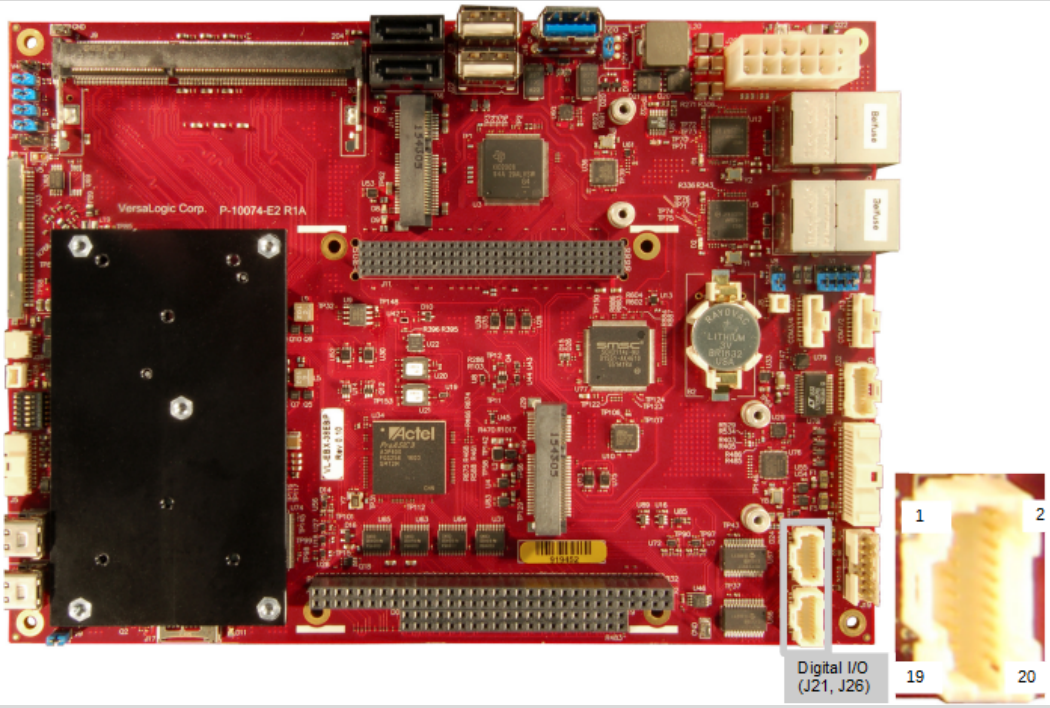


Table 14: J21/J26 I/O Connector Pinout

J21/J26 Pin	Signal	VL-CBR-2004B Terminal Block	Terminal Block Pin
1	Digital I/O 1/17	J1	5
2	Digital I/O 2/18		4
3	Digital I/O 3/19		3
4	Digital I/O 4/20		1
5	Ground		2
6	Digital I/O 5/21	J2	5
7	Digital I/O 6/22		4
8	Digital I/O 7/23		2
9	Digital I/O 8/24		1
10	Ground		3
11	Digital I/O 9/25	J3	5
12	Digital I/O 10/26		3
13	Digital I/O 11/27		2
14	Digital I/O 12/28		1
15	Ground		4
16	Digital I/O 13/29	J4	4
17	Digital I/O 14/30		3
18	Digital I/O 15/31		2
19	Digital I/O 16/32		1
20	Ground		5

DIO Guidelines

Consider the following guidelines when using the DIO lines.

VOLTAGE

The DIO lines are 3.3 V Low-voltage TTL (LVTTL) compatible DIOs capable of sourcing/sinking an absolute maximum of 25 mA of current. Level shifting or current limiting is necessary when connecting signals with different voltage rails.

CAUTION:

Do not connect the DIO signals to external +5 V devices; doing so will damage the DIO device and void the warranty.

POWER STATES

CPU power states will affect voltage rails driving DIO circuits as described below:

- The DIO power (which includes the pullup voltage) can be controlled (the same power used for the 8x GPIOs on the CBR-4005 paddleboard) using an FPGA register setting. By default, the DIOs power-down in sleep modes but can be configured to always stay on (along with the GPIOs).
- Power control during CPU power states on user devices connected to DIO lines is dependent on the application design. These external devices would likely remain powered unless a power-down mechanism is designed into the system.
- Care must be taken when powered DIO signals are connected to un-powered DIO signals. Significant voltage and current can be leaked from a powered system to an un-powered system causing unpredictable results. Current limiting and/or diode isolation can help.

CABLES

Cabling issues will affect the usable speed of DIO signals.

- These are single-ended drivers/receivers.
- Cabling crosstalk can be a problem with fast edge rates. The DIOs are slew-rate limited and have 50 Ω source terminators to minimize crosstalk and reflections.

ANALOG I/O (AIO)

Analog Inputs
A Linear Tech LTC1857 A/D device operates off a single 5V supply to provide eight 12-bit analog inputs. The LTC1857 provides eight single-ended input channels; or alternatively each even and odd analog channel "pair" (for example inputs 1 and 2 or 5 and 6) can be combined as differential inputs or you can also have combinations of both single-ended and differential channels. The converter has a 100 kilo-samples-per-second (ksps) sampling rate, with a 4 µs acquisition time and per-channel input ranges of 0 to 5V, ±5V, 0 to +10V and ±10V.

Analog Outputs
A Linear Tech LTC2634 D/A device is used to provide four single-ended 12-bit outputs. The converter has 5 µs per-channel update rate with a 0 to 4.096V output voltage range.

The Analog Output interface connects to a CBR-2004 paddle board via the J32 I/O connector. This is not considered a hot-plug interface and has no ESD protection.

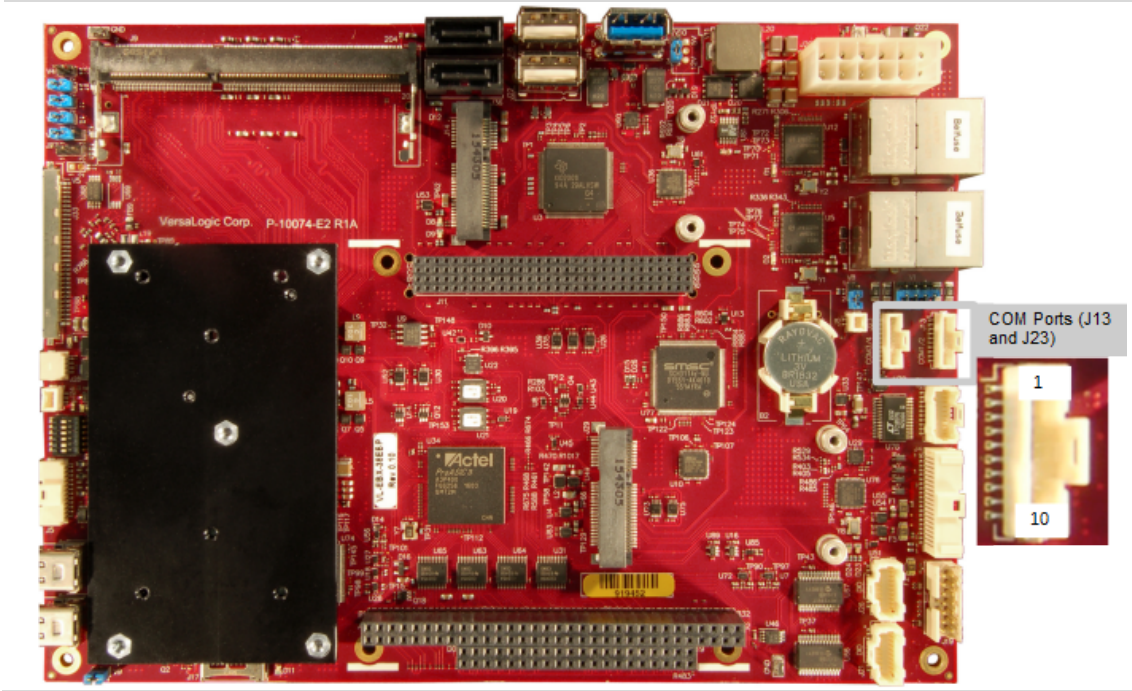
6 Serial Ports

The EBX-38 features four on-board 16550-based serial communications channels located at standard PC I/O addresses. The serial ports can be operated in RS-232 4-wire, RS-422, or RS-485 modes. IRQ lines are chosen in the BIOS Setup utility. Each COM port can be independently enabled, disabled, or assigned a different I/O base address in the BIOS setup utility.

Serial Port Connectors

The figure below shows the location and pin orientation of the two serial port connectors.

Figure 17. Location and Pin Orientation of Serial Port Connectors



SERIAL PORT CONNECTOR PINOUTS

Table 15: J13 COM1/COM2, J23 COM3/COM4 Connector Pinout

Pin	RS-232 Signal	RS-422/RS-485 Signal	Port
1	RTS1	TXD1_P	COM1 or COM3
2	TXD1#	TXD1_N	
3	CTS1	RXD1_P	
4	RXD1#	RXD1_N	
5	GND	GND	—
6	RTS2	TXD2_P	COM2 or COM4
7	TXD2#	TXD2_N	
8	CTS2	RXD2_P	
9	RXD2#	RXD2_N	
10	GND	GND	—

CABLING

An adapter cable, part number CBR-1014, is available for routing the J13 signals to 9-pin D-sub connectors. This is a 12-inch, Pico-Clasp 10-pin to two 9-pin D-sub connector cable.

If your application requires a custom cable, the following information will be useful:

EBX-38 Board Connector	Mating Connector
Molex 501331-1007	Molex 501330-1000

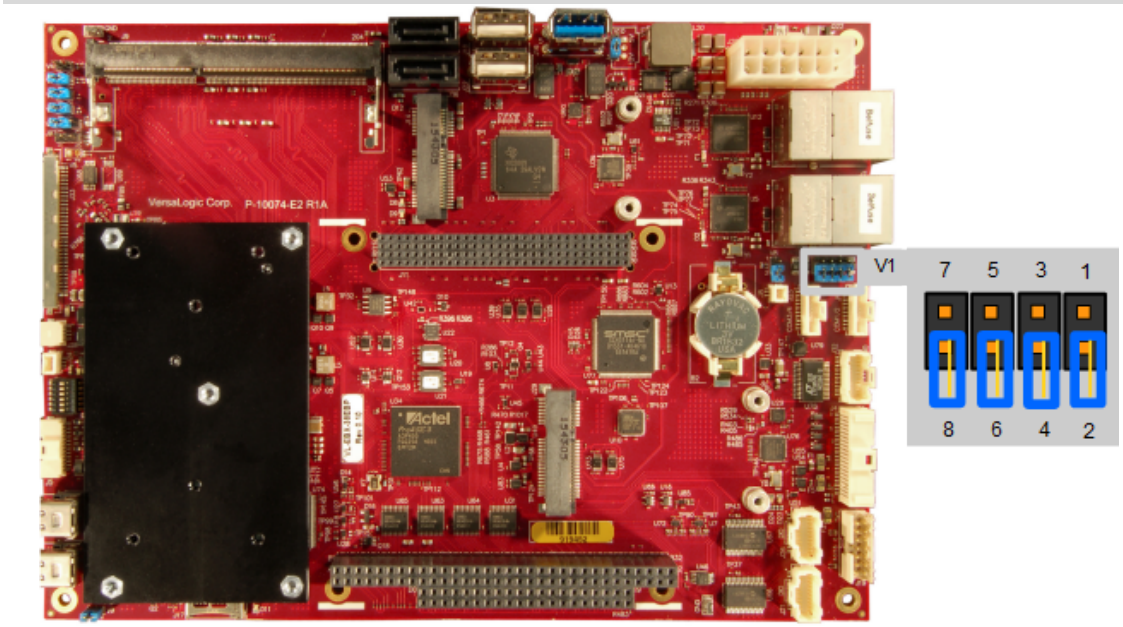
RS-485 MODE LINE DRIVER CONTROL

The transmit line driver can be automatically turned on and off based on data availability in the UART output FIFO (ADC mode). This mode can be enabled in the BIOS setup utility. The transmit line driver can alternatively always be enabled (Manual mode) in the BIOS Setup utility.

COM1/COM2/COM3/COM4 Hardware Configuration

Jumper block V1 [1-2] enables the RS-422/485 termination resistor for COM1. Jumper V1 [3-4] enables the RS-422/485 termination resistor for COM2. Jumper block V1 [5-6] enables the RS-422/485 termination resistor for COM3. Jumper V1 [7-8] enables the RS-422/485 termination resistor for COM4. The termination resistor should be enabled for an RS-422 or RS-485 endpoint station; it should be disabled for RS-232 and RS-485 non-endpoint receivers. Table 1 contains jumper configuration details.

Figure 18. COM1/COM2/COM3/COM4 End-point Termination Jumpers



7 Video Interfaces

The EBX-38 incorporates the Intel Gen-7 graphics core with four Execution Units and Turbo Boost. It supports two independent displays. It also supported formats including DirectX* 11, OpenGL 3, VP8, MPEG2, H.264, VC1, 2 HD streams (1080p@30fps), Flash and WMP support.

The analog (VGA), Dual Channel LVDS, and Mini DisplayPort video interfaces support Extended Desktop, Clone, and Twin display modes.

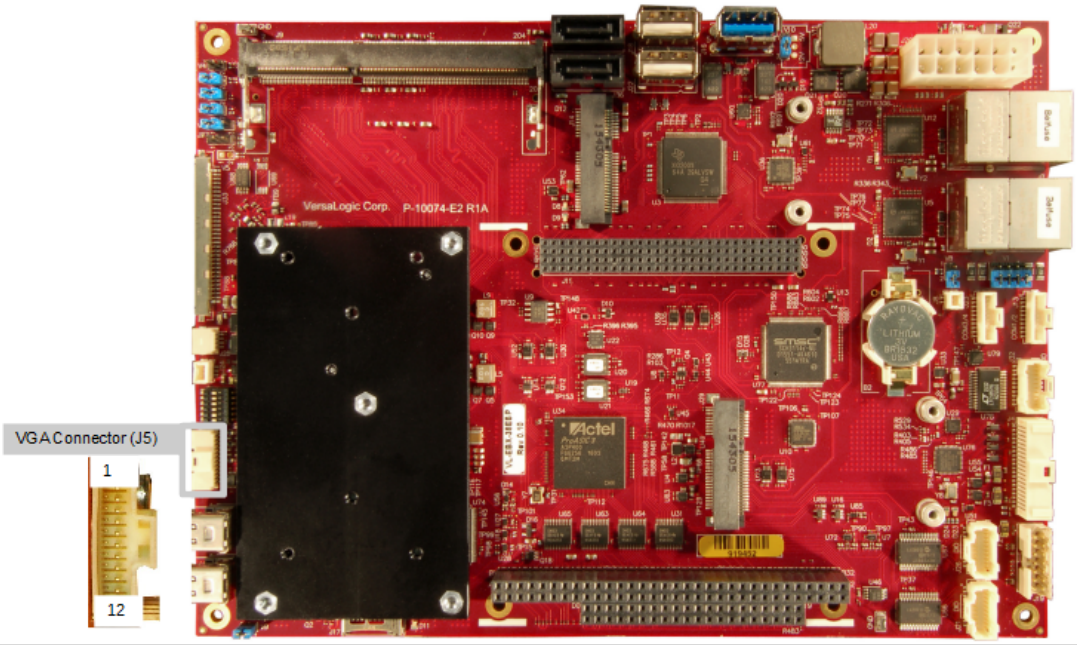
VGA Interface

The VGA port supports resolutions up to 1920 x 1080 at 60 Hz. This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

When the EBX-38 board is booted, the BIOS tests for a video monitor attached to the VGA port. If a monitor is not detected during this test, the VGA signals are disabled.

The figure below shows the location and pin orientation of the J5 VGA video output connector.

Figure 19. VGA Connector Location and Pin Orientation



This table lists the signals of the VGA video output connector.

Table 16: J5 VGA Video Output Pinout

Pin	Signal (Function)	DB-15 Pin
1	Ground	6
2	RED (Red video)	1
3	Ground	7
4	GREEN (Green video)	2
5	Ground	8
6	BLUE (Blue video)	3
7	Ground	5
8	HSYNC (Horizontal sync)	13
9	Ground	10
10	VSYNC (Vertical sync)	14
11	CRT_SCL (DDC data clock line)	15
12	CRT_SDA (DDC serial data line)	12

CABLING

An adapter cable, part number CBR-1204, is available to translate J5 into a standard 15-pin D-Sub VGA connector. This is a 12-inch, 12-pin Pico-Clasp to 15-pin VGA cable.

If your application requires a custom cable, the following information will be useful:

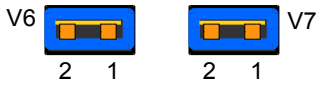
EBX-38 Board Connector	Mating Connector
Molex 501568-1207	Molex 501330-1200

LVDS Interface

Removal of jumper V9 disables J30 (the second Mini DisplayPort connector), and enables J33 Dual-Channel LVDS instead. The panel type select jumpers (V2, V3, V6, and V7) configure the EBX-38 for the LVDS display device. When choosing a display device, match the characteristics of your selection to the data in the first column of the table below. Set the panel resolution selection jumpers (V6 and V7) to match your display device's characteristics.

Table 17: LVDS Panel Types and Jumper Configurations

Panel Resolution	Jumper Configuration			
	V2	V3	V6	V7
800x600	IN	1-2	IN	IN
1024x768	IN	2-3	IN	OUT
1280x800	IN	2-3	OUT	IN
1920x1080	OUT	2-3	OUT	OUT

Supported Panel Characteristics	LVDS Signal Cable	Backlight Power Cable	V6/V7 Jumper Settings
▪ **Single channel** ▪ **18/24 bit** ▪ **800 x 600 (SVGA)**	VL-CBR-3003	VL-CBR-0601	
▪ **Single channel** ▪ **18/24 bit** ▪ **1024 x 768 (XGA)**	VL-CBR-3002	VL-CBR-0601	
▪ **Single channel** ▪ **18/24 bit** ▪ **1280 x 800 (WXGA)**	VL-CBR-3002	VL-CBR-0601	
▪ **Dual channel** ▪ **16.7M colors** ▪ **1920 x 1080 (HD 1080)**	VL-CBR-3001	——	

Integrator's Note:

Configure the J2, J3, V6, and V7 jumpers before connecting a display panel to the EBX-38. If any of the configuration jumpers are not properly set for the display device before power is turned on, no image will appear.

LVDS Panel Displays Tested with the EBX-38

The table below lists the LVDS panel displays tested with the EBX-38.

Table 18: LVDS Panel Displays Tested

Manufacturer	Model Number	Display Resolution	Display Size	LVDS Signal Cable
Sharp	LQ121S1LG42	800×600 SVGA	12.1 inches (31 cm)	VL-CBR-3003
Sharp	LQ150X1LG91	1024x768 XGA	15 inches (38 cm)	VL-CBR-3002

Sharp	LQ121K1LG52LCD	1280x800 (WXGA)	12.1 inches (31 cm)	VL-CBR-3002
LG	LM230WF3-SLD1	1920x1080 (HD 1080)	23 inches (58.4 cm)	VL-CBR-3001

LVDS Cables Available from VersaLogic

Table 19: LVDS Cables Available from VersaLogic

VersaLogic Part Number	Length	Channels	Function
VL-CBR-3001	20 inches	2	30-pin JAE to 30-pin JAE
VL-CBR-3002	20 inches	1	30-pin JAE to 20-pin Hirose
VL-CBR-3003	20 inches	1	30-pin JAE to 20-pin JAE

Mini DisplayPort Connectors

The Mini DisplayPort connectors J3 and J30 both support resolutions up to 2560 x 1440 at 24-bit.

DisplayPort consists of three interfaces:

- Main Link – transfers high-speed isochronous video and audio data
- Auxiliary channel – used for link management and device control; the EDID is read over this interface
- Hot Plug Detect – indicates that a cable is plugged in

Connector J3 DisplayPort interface also supports:

- Audio signaling (Audio is disabled by default in BIOS Setup so it would need to be enabled before use.)
- DP++ mode allowing connection to an HDMI device through a passive adapter. "Passive" means that the adapter does not require external power (because it uses the DP port's 3.3 V power) and it does not require software drivers.

The figure below shows the locations of the 20-pin Mini DisplayPort connectors. Table 20 lists the pinout of the J3 Mini DisplayPort0 connector and J30 Mini DisplayPort1 connector.

Figure 20. Location of the Mini DisplayPort Connectors

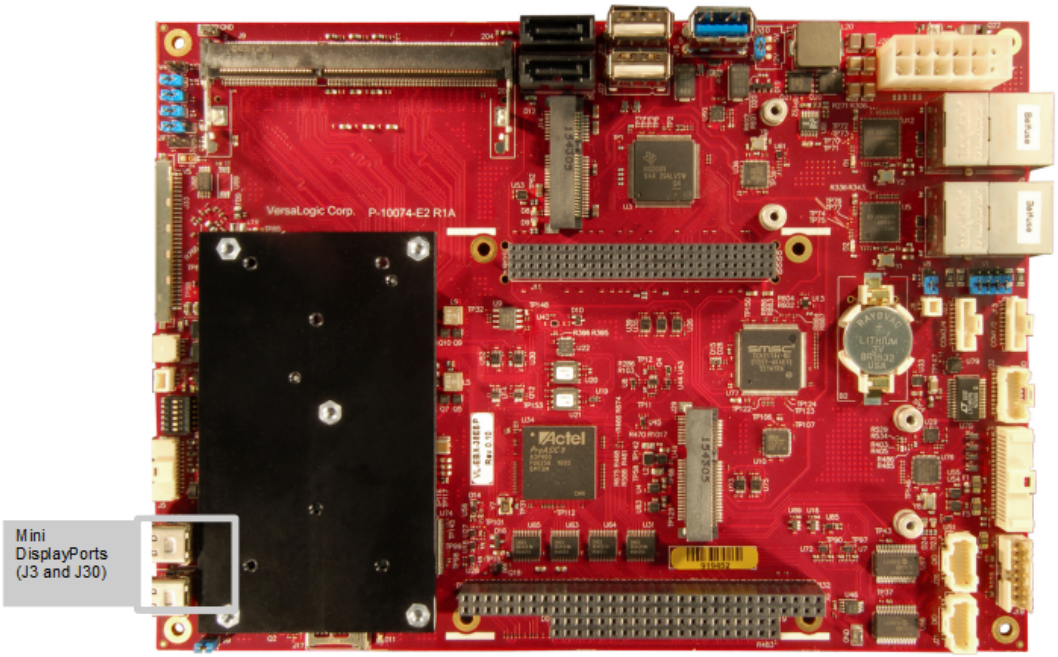


Table 20: J3/J30 Mini DisplayPort Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	HOT PLUG DETECT
3	ML_LANE0_P	4	CONFIG 1
5	ML_LANE0_N	6	CONFIG 2
7	GND	8	GND
9	ML_LANE1_P	10	ML_LANE3_P
11	ML_LANE1_N	12	ML_LANE3_N
13	GND	14	GND
15	ML_LANE2_P	16	AUX_CH_P
17	ML_LANE2_N	18	AUX_CH_N
19	RTN	20	DP_POWER

Console Redirection

The EBX-38 can be configured for remote access by redirecting the console to a serial communications port. The BIOS setup utility and some operating systems (such as MS-DOS) can use this console for user interaction. The default settings for the redirected console are as follows:

- 115,200 baud rate
- 8 data bits, no parity
- 1 stop bit
- No parity
- No flow control

8 Network Interfaces

The EBX-38 provides two on-board Intel I210-IT Gigabit Ethernet controllers. The controllers provide a standard Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. The I210-IT Ethernet controller auto-negotiates connection speed. Drivers are available to support a variety of operating systems.

ETHERNET CONNECTORS

The J1/J7 connectors provide access to the Ethernet ports 0 and 1. The connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage. The figure below shows the location and pin orientation of the Ethernet connector.

Figure 21. Location for the J1/J7 Ethernet Connectors

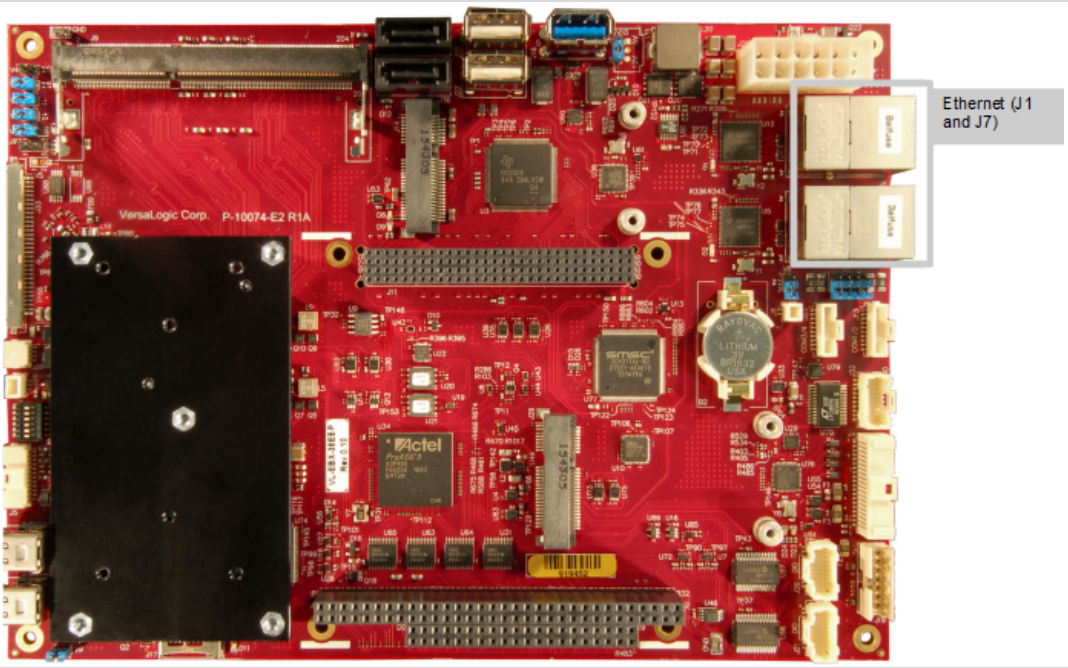


Table 21: Ethernet Connector Pinout

J1 and J7 - (XMRJ45MGL2RA)	10/100 Signals	10/100/1000 Signals
9	+ Auto Switch (can be either Tx or Rx)	BI_DA+
10	- Auto Switch (can be either Tx or Rx)	BI_DA-
7	+ Auto Switch (can be either Tx or Rx)	BI_DB+
5	+ Auto Switch (can be either Tx or Rx)	BI_DC+
6	- Auto Switch (can be either Tx or Rx)	BI_DC-
8	- Auto Switch (can be either Tx or Rx)	BI_DB-
3	+ Auto Switch (can be either Tx or Rx)	BI_DD+
4	- Auto Switch (can be either Tx or Rx)	BI_DD-
1	Ground for built in capacitors	
2	Common Center Tap for BIAS voltage	
11	Green LED Anode	
12	Green LED Cathode	
13	Yellow LED Anode	
14	Yellow LED Cathode	

CABLING

Two RJ-45 connector cables MagJacks which are CAT5E performance rated.

ON-BOARD ETHERNET STATUS LEDS

On-board status LEDs are provided for both Ethernet ports:

- J1 (green LED) provides status for Ethernet port 0
- J7 (green LED) provides status for Ethernet port 1

Figure 22. Location of Ethernet Status LEDs

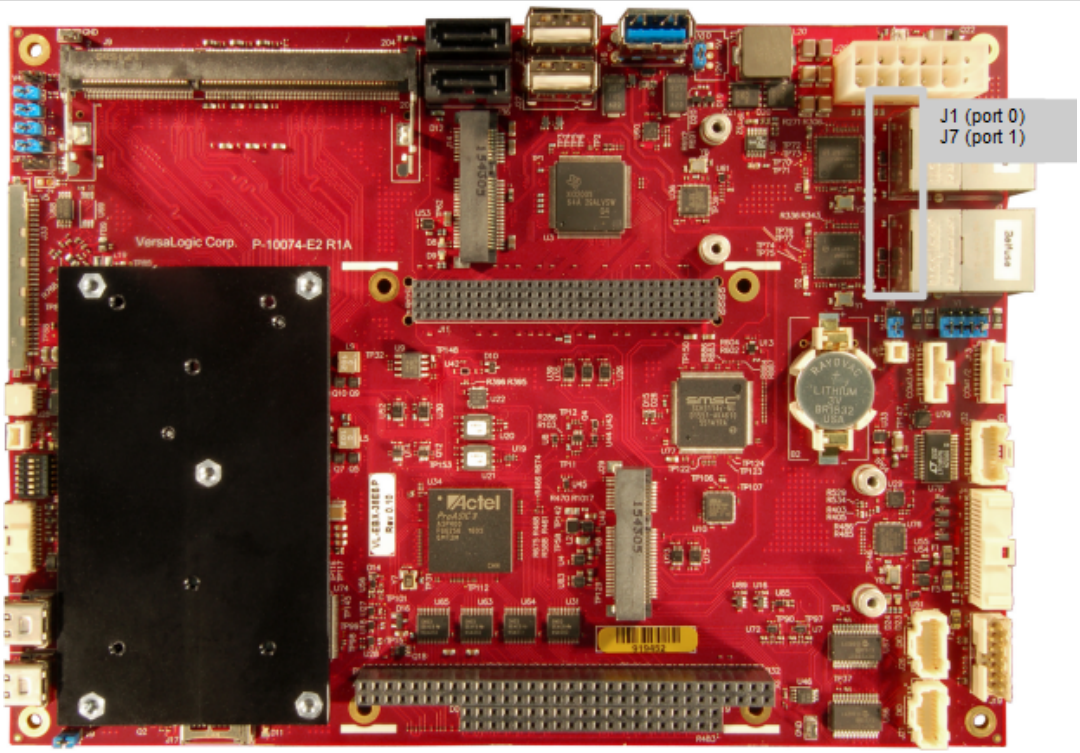


Table 22: Ethernet Status LEDs

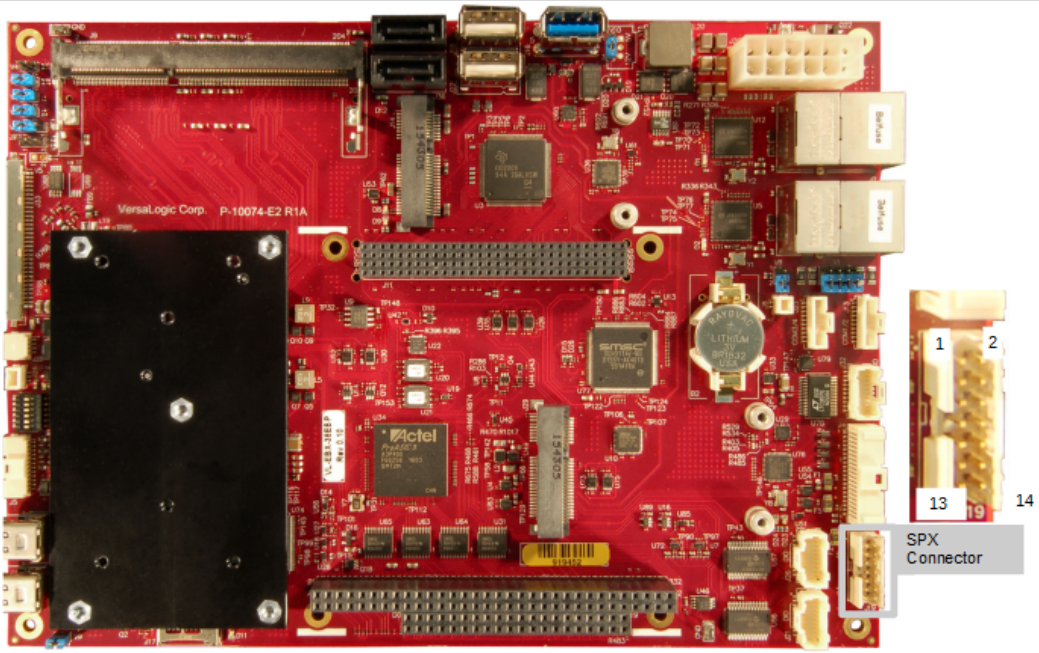
LED	Ref Des	State	Description
Green (Activity or link/status) On left	J1(Port 0) J7 (Port 1)	On	Cable connected (pulses with activity)
		Off	Cable not connected
Yellow (Activity or link/status) On right	J1(Port 0) J7 (Port 1)	1Gbit speed indicator	Speed indicator
		10/100	

SPX™ Expansion Bus

Up to four serial peripheral expansion (SPX) devices can be attached to the EBX-38 at connector J19 using a CBR-1401 or 1402 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: CLK, MISO, and MOSI, as well as four chip selects, SS0#, SS1#, SS2#, and SS3# and INT#. The +5 V power provided to pin 1 of the SPX connector is protected by a 1 A resettable fuse.

The figure below shows the location of the SPX connector.

Figure 23. J19 SPX Connector Location and Pin Configuration



The table below lists the pinout of the SPX connector.

Table 23: SPX Connector Pinout

Pin	Signal	Function
1	VCC	5V Power (Fused from S0 power in this product)
2	SCLK	SPX Clock
3	GND	Ground
4	MISO	Serial Data input (Master In Slave Out)
5	GND	Ground
6	MOSI	Serial Data output (Master Out Slave In)
7	GND	Ground
8	SS0#	Chip Select 0 (low true)
9	SS1#	Chip Select 1 (low true)
10	SS2#	Chip Select 2 (low true)
11	SS3#	Chip Select 3 (low true)
12	GND	Ground
13	INT#	Interrupt input (low true)
14	VCC	5V Power (Fused from S0 power in this product)

SPI is, in its simplest form, a three wire serial bus. One signal is a clock, driven only by the permanent master device on-board. The others are Data In and Data Out with respect to the master. The SPX implementation on the EBX-38 board supports chip selects. The master device initiates all SPI transactions. A slave device responds when its chip select is asserted and it receives clock pulses from the master. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

The SPI clock is derived from a 33 MHz PCI clock and can be software-configured to operate at the following frequencies:

- 8.25 MHz (33 MHz/4)
- 4.125 MHz (33 MHz/8)
- 2.0625 MHz (33 MHz/16)
- 1.03125 MHz (33 MHz/32)

CABLING

Adapter cables, part number CBR-1401(Six inch) or CBR-1402 (Twelve inch), are available.

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers several SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2 inches x 3.775 inches) that can mount on the PC/104 and PC/104-*Plus* stack, using standard PC/104 stand-offs, or up to two feet away from the base board. For more information, contact VersaLogic at info@VersaLogic.com.

PC/104-*Plus* Expansion Bus

The EBX-38 provides a legacy stack-up PCI connector at locations J11(for PCI) and J10A and J10B (for ISA) on the top side of the board for PC/104-*Plus* (PCI +ISA) as well as PCI-104 (PCI only) and PC/104 (ISA only) expansion modules.

Figure 2 on page 2 shows the locations of these connectors.

The following table lists the maximum PC/104-*Plus* slot current rating on the EBX-38. This is the aggregate power available to both the PCI and ISA connectors. ISA does not use +3.3V power, so all of the +3.3 V power is available for the PCI connector.

Table 24: PC/104-*Plus* Connectors Maximum Current

Voltage	Maximum Current
+5 V	4.0 A
+3.3 V	3.0 A
+12 V	1.0 A
–12 V	0.5 A

ISA Bus (on PC/104-*Plus* and PC/104 Expansion Modules)

Refer to the ISA sections of the PC/104-*Plus* Specification for a complete description of this interface.

The EBX-38 implements the ISA bus on PC/104-*Plus* and PC/104 expansion modules using an LPC-to-ISA bridge implemented in the FPGA. This LPC-to-ISA bridge supports all features except the following:

- The ISA bus must not be mastered by an external module. The EBX-38 is always the bus master. The MASTER signal on pin D17 of J10 is not connected.
- The REFRESH output signal on B19 of J10 is not supported; it is pulled up to a high logic level.
- DMA is not supported. The seven DACKx outputs on pins B15, B17, B26, D8, D10, D12, and D14 on J10 are pulled up to a high logic level. The seven DRQx inputs on pins B6, B16, B18, D9, D11, D13, and D15 on J10 are not connected. The Terminal Count (TC) output on pin B27 of J10 is pulled low.
- –5.0V power is not provided on J10 pin B5. This pin is not connected.

Most PC/104-*Plus* (PCI +ISA) or PC/104 (ISA only) expansion modules will work, but be sure to check the requirements of your PC/104 card against the list above.

ISA I/O Support

Both 8-bit and 16-bit I/O cycles are supported, but for 16-bit cycles the PC/104 (ISA) module must be 16-bit capable and must assert IOCS16#.

The next table lists the I/O ranges available on the ISA bus unless there is a device claiming the range on the LPC or PCI bus. The FPGA on the EBX-38 uses I/O addresses 0xC80-0xCCF and, if enabled, the four COM ports that can be configured in the BIOS Setup utility to map to various address ranges will be blocked by the FPGA from ISA I/O accesses. The FPGA always blocks 0x2E/0x2F and 0xC00 – 0xC7F for the SCH3114 Index/Data and Runtime Registers.

By default, the four COM ports in the FPGA are enabled and occupy the I/O address ranges of 0x3F8-0x3FF, 0x2F8-0x2FF, 0x3E8-0x3EF, and 0x2E8-0x2EF. The following are the I/O address ranges available on the ISA bus when the BIOS is configured to factory defaults.

Table 25: Available ISA Bus I/O Ranges

▪ 0x0 – 0x1F	▪ 0x43 – 0x4F	▪ 0x93 – 0x9F	▪ 0x3BC – 0x3BF
▪ 0x22 – 0x23	▪ 0x53 – 0x60	▪ 0xA2 – 0xA3	▪ 0x3E0-0x3FF,
▪ 0x26 – 0x27	▪ 0x62	▪ 0xA6 – 0xA7	▪ 0x480 – 0x4CF
▪ 0x2A – 0x2B	▪ 0x64	▪ 0xAA – 0xAB	▪ 0x4D2 – 0x4FF
▪ 0x32 – 0x33	▪ 0x66	▪ 0xAE – 0xAF	▪ 0x600 – 0xBFF
▪ 0x36 – 0x37	▪ 0x68 – 0x70	▪ 0xB6 – 0xB7	▪ 0xCD0 – 0xCF8
▪ 0x3A – 0x3B	▪ 0x78 – 0x7F	▪ 0xBA – 0xBB	▪ 0xCFA – 0xCFB
▪ 0x3E – 0x3F	▪ 0x90 – 0x91	▪ 0xBE-0x3AF	▪ 0xD00 – 0xFFF

Assuming the COM ports are disabled, the available I/O base addresses for COM ports on the ISA bus are as follows:

▪ 0x200	▪ 0x228	▪ 0x338
▪ 0x208	▪ 0x238	▪ 0x3E8
▪ 0x220	▪ 0x2E8	▪ 0x3F8
▪ 0x2F8		

Each COM port in the FPGA that is enabled will use one of these I/O base addresses and, in that case, that 8 byte I/O range will not be available on the ISA bus. PCI devices may be assigned I/O space, but that usually occurs at I/O address 0x1000 or higher so as to not conflict with legacy I/O devices.

ISA MEMORY SUPPORT

The following memory addresses are available on the ISA bus:

- 0xA0000 – 0xB7FFF

ISA IRQ SUPPORT

The following IRQs are supported on the ISA bus:

▪ IRQ3	▪ IRQ9
▪ IRQ4	▪ IRQ10
▪ IRQ5	▪ IRQ11
▪ IRQ6	▪ IRQ12
▪ IRQ7	▪ IRQ15

Each of the IRQs must be enabled in the BIOS Setup utility before they can be used. (All are disabled by default.)

Because ISA IRQ sharing is not supported, IRQs may not be available to the ISA bus due to operating system limitations.

PCI BUS (ON PC/104-*PLUS* EXPANSION MODULES)

Refer to the PCI sections of the PC/104-*Plus* Specification for a complete description of this interface.

Make sure to correctly configure the PCI slot position jumpers on each PC/104-*Plus* or PCI-104 module appropriately.

The BIOS automatically allocates I/O, memory, and interrupt resources.

10 System Resources and Maps

Refer to the *EBX-38 Programmer's Reference Manual* for the following information:

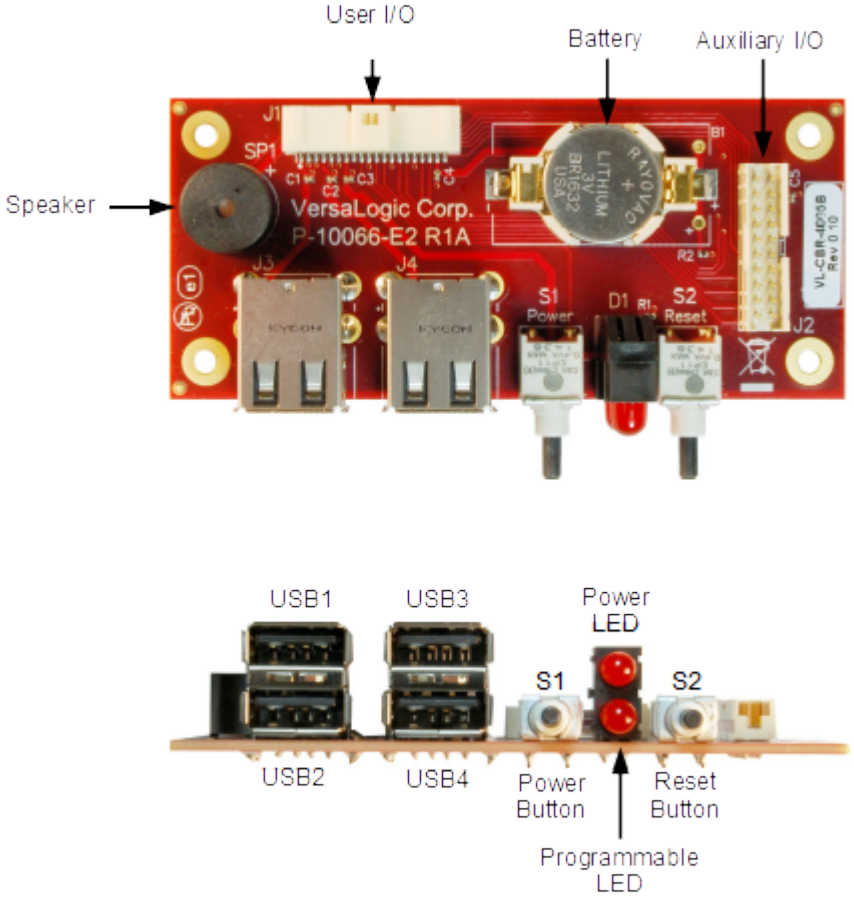
- Memory map
- IRQ map
- I/O map
- FPGA register map
- FPGA register descriptions
- Programming information for certain hardware interfaces.

CBR-4005B Paddleboard

CBR-4005B Connectors and Indicators

The figure below shows the locations of the connectors, switches, and LEDs on the CBR-4005B paddleboard.

Figure 24. CBR-4005B Connectors, Switches, and LEDs



USER I/O CONNECTOR

This figure shows the location and pin orientation of the user I/O connector.

Figure 25. Location and Pin Orientation of the User I/O Connector

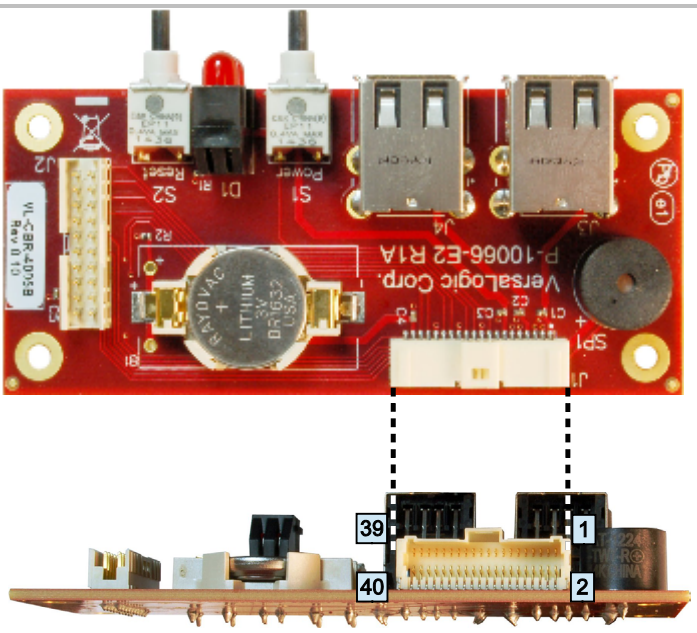


Table 26: User I/O Connector Pinout

Pin	Signal	Pin	Signal
1	+5 V	2	GND
3	USB1_P	4	USB2_P
5	USB1_N	6	USB2_N
7	+5V	8	GND
9	USB3_P	10	USB4_P
11	USB3_N	12	USB4_N
13	+3.3 V	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	Reserved	22	V_BATT
23	Reserved	24	V_BATT_RETURN
25	GND	26	GND
27	FPGA GPIO1	28	FPGA GPIO2
29	FPGA GPIO3	30	FPGA GPIO4
31	GND	32	GND
33	FPGA GPIO5	34	FPGA GPIO6
35	FPGA GPIO7	36	FPGA GPIO8
37	+3.3 V	38	GND
39	ETH0 LED	40	ETH1 LED

CABLING

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EBX-38. This is a 12-inch, Pico-Clasp 40-pin to 40-pin cable

If your application requires a custom cable, the following information will be useful:

CBR-4005B Board Connector	Mating Connector
Molex 501571-4007	Molex 501189-4010

ON-BOARD BATTERY

CAUTION:

To prevent shorting, premature failure or damage to the Lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The Lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of the battery in fire. Dispose of used batteries promptly.

Nominal battery voltage is 3.0 V. If the voltage drops below 2.7 V, contact the factory for a replacement. The life expectancy under normal use is approximately five years.

AUXILIARY I/O CONNECTOR

The figure below shows the location and pin orientation of the auxiliary I/O connector.

Figure 26. Location and Pin Orientation of Auxiliary I/O Connector

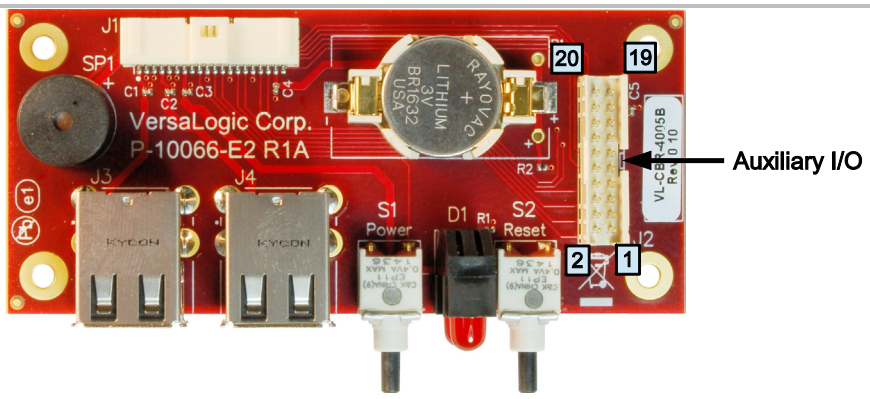
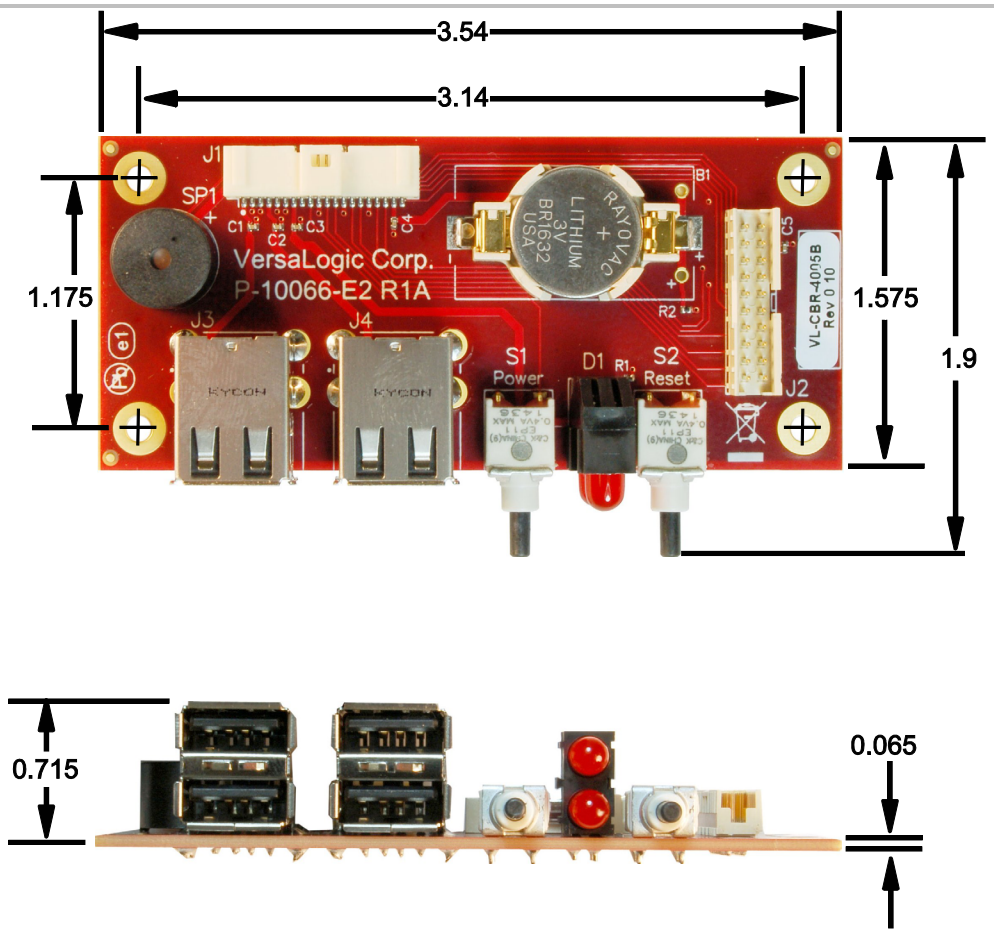


Table 27: Auxiliary I/O Connector Pinout

Pin	Signal	Pin	Signal
1	Reserved	2	V_BATT
3	Reserved	4	V_BATT_RETURN
5	GND	6	GND
7	FPGA GPIO1	8	FPGA GPIO2
9	FPGA GPIO3	10	FPGA GPIO4
11	GND	12	GND
13	FPGA GPIO5	14	FPGA GPIO6
15	FPGA GPIO7	16	FPGA GPIO8
17	+3.3 V	18	GND
19	Ethernet Port 0 LED	20	Ethernet Port 1 LED

Figure 27. CBR-4005B Dimensions and Mounting Holes



Digital I/O (Using VL-CBR-2005A x2)

Two Microchip MCP23S17 digital I/O expander devices are used to provide thirty-two I/O lines. The digital lines are grouped into two sets (per two devices) of 16-bit bi-directional ports. Within each MCP23S17 device, the 16-bit I/O port functionality consists of two 8-bit ports, and can be configured to operate in 8-bit or 16-bit mode and controlled by software. The digital I/O lines are powered up in the input mode and make an excellent choice for industrial LVTTL interfacing. All of the I/O pins support +3.3V signaling.

The Digital I/O interface connects to two CBR-2005 (Cable and Paddleboard Assembly) via the J21 and J26 I/O connectors.

Table 28. Digital I/O Using VL-CBR-2005A 1

Pin	Signal	Description	Pin	Signal	Description
1	DIO1/DIO17	Digital I/O	2	DIO2/DIO18	Digital I/O
3	DIO3/DIO19	Digital I/O	4	DIO4/DIO20	Digital I/O
5	DGND	Digital Signal Ground	6	DIO5/DIO21	Digital I/O
7	DIO6/DIO22	Digital I/O	8	DIO7/DIO23	Digital I/O
9	DIO8/DIO24	Digital I/O	10	DGND	Digital Signal Ground
11	DIO9/DIO25	Digital I/O	12	DIO10/DIO26	Digital I/O
13	DIO11/DIO27	Digital I/O	14	DIO12/DIO28	Digital I/O
15	DGND	Digital Signal Ground	16	DIO13/DIO29	Digital I/O
17	DIO14/DIO30	Digital I/O	18	DIO15/DIO31	Digital I/O
19	DIO16/DIO32	Digital I/O	20	DGND	Digital Signal Ground

Table 29. Digital I/O Using VL-CBR-2005A 2

J#-Pin#	CBR-2004B Signal	EBX-38 Description	J#-Pin#	CBR-2004B Signal	EBX-38 Description
J1-5	DIO1	Digital I/O Ch. 1	J1-5	DIO1	Digital I/O Ch. 17
J1-4	DIO2	Digital I/O Ch. 2	J1-4	DIO2	Digital I/O Ch. 18
J1-3	DIO3	Digital I/O Ch. 3	J1-3	DIO3	Digital I/O Ch. 19
J1-2	DGND1	Digital Signal Ground	J1-2	DGND1	Digital Signal Ground
J1-1	DIO4	Digital I/O Ch. 4	J1-1	DIO4	Digital I/O Ch. 20
J2-5	DIO5	Digital I/O Ch. 5	J2-5	DIO5	Digital I/O Ch. 21
J2-4	DIO6	Digital I/O Ch. 6	J2-4	DIO6	Digital I/O Ch. 22
J2-3	DGND2	Digital Signal Ground	J2-3	DGND2	Digital Signal Ground
J2-2	DIO7	Digital I/O Ch. 7	J2-2	DIO7	Digital I/O Ch. 23
J2-1	DIO8	Digital I/O Ch. 8	J2-1	DIO8	Digital I/O Ch. 24
J3-5	DIO9	Digital I/O Ch. 9	J3-5	DIO9	Digital I/O Ch. 25
J3-4	DGND3	Digital Signal Ground	J3-4	DGND3	Digital Signal Ground
J3-3	DIO10	Digital I/O Ch. 10	J3-3	DIO10	Digital I/O Ch. 26
J3-2	DIO11	Digital I/O Ch. 11	J3-2	DIO11	Digital I/O Ch. 27
J3-1	DIO12	Digital I/O Ch. 12	J3-1	DIO12	Digital I/O Ch. 28
J4-5	DGND4	Digital Signal Ground	J4-5	DGND4	Digital Signal Ground
J4-4	DIO13	Digital I/O Ch. 13	J4-4	DIO13	Digital I/O Ch. 29
J4-3	DIO14	Digital I/O Ch. 14	J4-3	DIO14	Digital I/O Ch. 30
J4-2	DIO15	Digital I/O Ch. 15	J4-2	DIO15	Digital I/O Ch. 31
J4-1	DIO16	Digital I/O Ch. 16	J4-1	DIO16	Digital I/O Ch. 32

Analog I/O (Using VL-CBR-2004A)

A Linear Tech LTC1857 A/D device operates off a single 5V supply to provide eight 12-bit analog inputs. The LTC1857 provides eight single-ended input channels; or alternatively each even and odd analog channel "pair" (for example inputs 1 and 2 or 5 and 6) can be combined as differential inputs or you can also have combinations of both single-ended and differential channels.

A Linear Tech LTC2634 D/A device is used to provide four single-ended 12-bit outputs. The converter has 5 µs per-channel update rate with a 0 to 4.096V output voltage range.

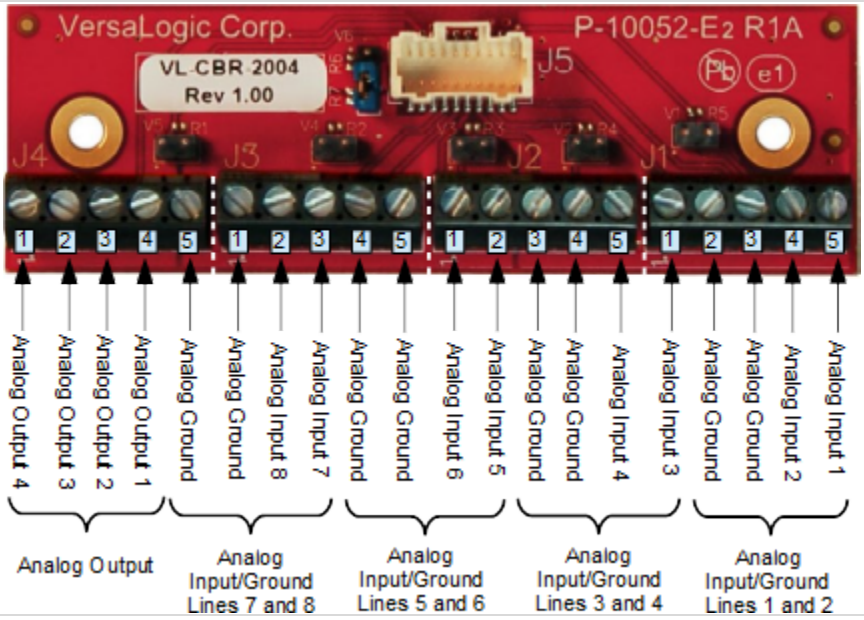
The Analog Output interface connects to a CBR-2004 paddle board via the J32 I/O connector.

Note: The V6 jumper on the paddleboard needs to be on pins 2-3 (connecting GND3 to GND2) for Analog I/O use.

Table 30. Analog I/O Using VL-CBR-2004A

Pin	Signal	Description	Pin	Signal	Description
1	ADC_CH1	Analog Input	2	ADC_CH2	Analog Input
3	AGND	Analog Signal Ground	4	AGND	Analog Signal Ground
5	ADC_CH3	Analog Input	6	ADC_CH4	Analog Input
7	AGND	Analog Signal Ground	8	AGND	Analog Signal Ground
9	ADC_CH5	Analog Input	10	ADC_CH6	Analog Input
11	AGND	Analog Signal Ground	12	AGND	Analog Signal Ground
13	ADC_CH7	Analog Input	14	ADC_CH8	Analog Input
15	AGND	Analog Signal Ground	16	AGND	Analog Signal Ground
17	DAC_OUT1	Analog Output	18	DAC_OUT2	Analog Output
19	DAC_OUT3	Analog Output	20	DAC_OUT4	Analog Output

Figure 28. CBR-2004 Analog I/O Connectors



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Thermal Considerations 13

This chapter discusses the following topics related to thermal issues:

- Selecting the correct thermal solution for your application (begins below)
- EBX-38 thermal characterization (begins on page 64)
- Installing the passive (HDW-406 heat sink) and active (HDW-407 fan) thermal solutions available from VersaLogic (begins on page 60)

Selecting the Correct Thermal Solution for Your Application

This section provides guidelines for the overall system thermal engineering effort.

HEAT PLATE

The heat plate supplied with the Viper is the basis of the thermal solution. The heat plate draws heat away from the CPU chip as well as other critical components such as the power supply / management unit (PMIC), the 3.3V Regulator for the board I/O, and the PCIe Switch interfaces. Other components rely on the ambient air temperature being maintained at or below the maximum specified 85 ºC.

The heat plate is designed with the assumption that the user's thermal solution will maintain the top surface of the heat plate at 90 ºC or less. If that temperature threshold is maintained, the CPU (and the other noted components) will remain safely within their operating temperature limits.

CAUTION:

By itself, the heat plate is not a complete thermal solution. Integrators should either implement a thermal solution using the accessories available from VersaLogic or develop their own thermal solution that attaches to the heat plate, suitable for environments in which the EBX-38 will be used. As stated above, any thermal solution must be capable of keeping the top surface of the heat place at or below 90 ºC and the air surrounding the components in the assembly at or below 85 ºC.

The heat plate is permanently affixed to the Viper and must not be removed. Removal of the heat plate voids the product warranty. Attempting to operate the Viper without the heat plate voids the product warranty and can damage the CPU.

SYSTEM-LEVEL CONSIDERATIONS

The EBX-38 thermal solutions – either the HDW-406 heat sink alone or with the HDW-407 fan – are part of the larger thermal system of the application. Other PC/104 boards stacked above the Viper and any other nearby heat sources (power supplies or other circuits), all contribute to how the EBX-38 will perform from a thermal standpoint.

The ambient air surrounding the EBX-38 needs to be maintained at 85 ºC or below. This can prove to be challenging depending on how and where the EBX-38 is mounted in the end user system. Standard methods for addressing this requirement include the following:

- Provide a typical airflow of 100 linear feet per minute (LFM) / 0.5 linear meters per second (as described beginning on page 64) within the enclosure
- Position the EBX-38 board to allow for convective airflow
- Lower the system level temperature requirement as needed

The decision as to which thermal solution to use can be based on several factors including (but not limited to) the following:

- Number of CPU cores in the SoC (single, dual, or quad)
- CPU core program utilization
- Temperature range within which the EBX-38 will be operated
- Air movement (or lack of air movement)
- Video processing intensity
- Memory access demands
- High speed I/O usage (PCIe, USB 3.0, SATA usage)

Most of these factors involve the demands of the user application on the EBX-38 and cannot be isolated from the overall thermal performance. Due to the interaction of the user application, the Viper thermal solution, and the overall environment of the end system, thermal performance cannot be rigidly defined.

CPU THERMAL TRIP POINTS

The CPU cores in the Viper have their own thermal sensors. Coupled with these sensors are specific reactions to four thermal trip points. The table below describes the four thermal trip points.

Table 31. CPU Thermal Trip Points

Trip Point	Description
Active (Note 1)	The fan is turned on when this temperature is reached
Passive (Note 2)	At this temperature, the CPU cores throttle back to a lower speed. This reduces the power draw and the temperature.
Critical (Note 3)	At this temperature, the operating system typically puts the board into a sleep or other low-power state.
Maximum core temperature	The CPU turns itself off when this temperature is reached. This is a fixed trip point and cannot be adjusted.

Notes:
1. The default value in the BIOS Setup utility for this trip point is 55 ºC.
2. The default value in the BIOS Setup utility for this trip point is 105 ºC.
3. The default value in the BIOS Setup utility for this trip point is 110 ºC.

These trip points allow maximum CPU operational performance while maintaining the lowest CPU temperature possible. The long-term reliability of any electronic component is degraded when it is continually run near its maximum thermal limit. Ideally, the CPU core temperatures would be kept well below 100 ºC with only brief excursions above.

CPU temperature monitoring programs are available to run under both Windows and Linux. The table below lists some of these hardware monitoring programs.

Table 32. Temperature Monitoring Programs

Operating System	Program Type	Description
Windows	Core Temperature	http://www.alcpu.com/CoreTemp/
	Hardware Monitor	http://www.cpuid.com/softwares/hwmonitor.html
	Open Hardware Monitor	http://openhardwaremonitor.org/
Linux	lm-sensors	http://en.wikipedia.org/wiki/Lm_sensors

THERMAL SPECIFICATIONS, RESTRICTIONS, AND CONDITIONS

Graphical test data is in the section titled EBX-38 Thermal Characterization, beginning on page 64. Refer to that section for the details behind these specifications. These specifications are the thermal limits for using the EBX-38 with one of the defined thermal solutions.

Due to the unknown nature of the entire thermal system, or the performance requirement of the application, VersaLogic cannot recommend a particular thermal solution. This information is provided for user guidance in the design of their overall thermal system solution.

Table 33. Absolute Minimum and Maximum Air Temperatures

Board	With Heat Plate	With Heat Sink (HDW-406)	With Heat Sink + Fan (HDW-413)
VL-EPMe-42EAP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C
VL-EPMe-42EBP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C
VL-EPMe-42ECP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C

OVERALL RESTRICTIONS AND CONDITIONS

- Ranges shown assume less than 90% CPU utilization.
- Keep the maximum CPU core temperature below 100ºC.
- The ambient air surrounding the EBX-38 needs to be maintained at 85 ºC or below. This includes the space between this CPU board and any board it is stacked on top of it. Included is the space beneath an installed Mini PCIe expansion board and the installed SODIMM. A recommended overall air flow of 100 Linear Feet per Minute (LFM) / 0.5 Linear Meters per Second (LMS) addresses this requirement. If this air flow is not provided, other means to keep the adjacent air at 85 ºC or below must be implemented.

HEAT PLATE ONLY RESTRICTIONS AND CONDITIONS:

- The heat plate must be kept below 90 °C. This applies to a heat plate mounted directly to another surface.

HEAT SINK ONLY CONSIDERATIONS:

- At 85°C air temperature and 90% CPU utilization, there will be little – if any – thermal margin to a CPU core temperature of 100 °C or the passive trip point (see test data). If this is the use case, consider adding a fan or other additional air flow.

HEAT SINK WITH FAN CONSIDERATIONS:

- The heat sink and fan combination cools the CPU when it is running in high temperature environments, or when the application software is heavily utilizing the CPU or video circuitry. The fan assists in cooling the heat sink and provides additional air movement within the system.

Integrator's Note:

The ambient air surrounding the EBX-38 needs to be maintained at 85 ºC or below.

EBX-38 Thermal Characterization

The EBX-38 board underwent the following thermal characterization tests:

- Test Scenario 1: Single core EBX-38EAP with passive and active thermal solutions
- Test Scenario 2: Dual core EBX-38EBP with passive and active thermal solutions
- Test Scenario 3: Quad core EBX-38ECP with passive and active thermal solutions
- The table below describes the thermal testing setup for the board.

Table 34. EBX-38 Thermal Testing Setup

Hardware Configuration	EBX-38 (Viper) core CPU with: ▪ 8 GB of DDR3 DRAM (VersaLogic part number VL-MM9-4EBN) ▪ HDW-406 (passive heat sink) ▪ HDW-407 (heat sink fan) ▪ One attached DisplayPort device ▪ Two RS-232 ports in loopback configuration ▪ Two active Ethernet ports ▪ Three USB 2.0 ports in loopback configuration
BIOS	▪ IP-1081 ▪ Passive thermal trip point setting: 105 ºC ▪ Critical thermal trip point setting: 110 ºC
Operating System	▪ Microsoft Windows* 10 Enterprise
Test Software	▪ Passmark* BurnIn Test v8.1 - CPU utilization ~90% ▪ Intel Thermal Analysis Tool* (TAT) v6.0.1007 - Primarily used to read the CPU core temperature
Test Environment	▪ Thermal chamber

The test results reflect the test environment within the temperature chamber used. This particular chamber has an airflow of about 0.5 meters per second (~100 linear feet per minute). Thermal performance can be greatly enhanced by increasing the overall airflow beyond 0.5 meters per second.

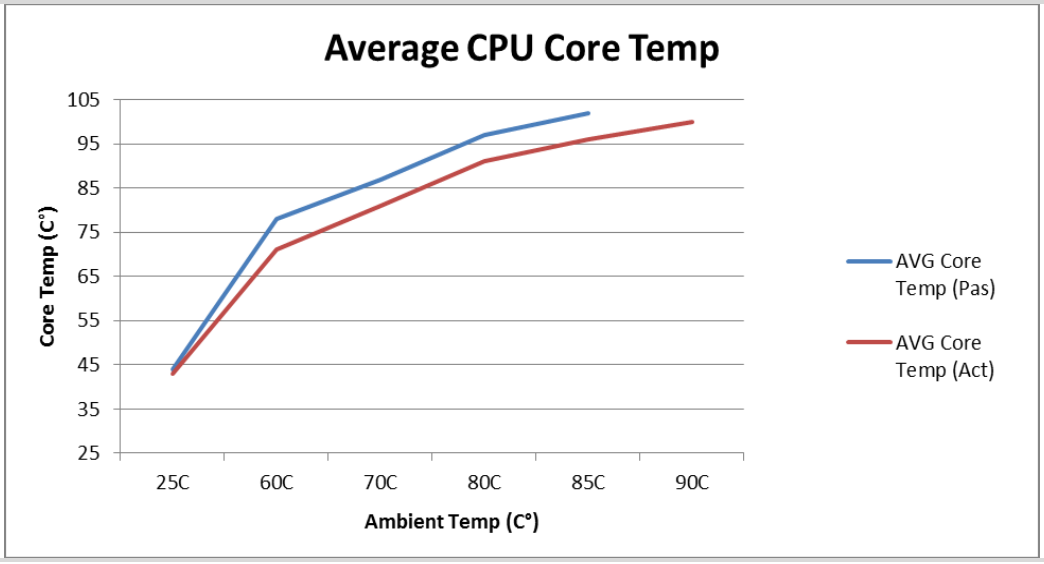
The system power dissipation is primarily dependent on the application program - that is, its use of computing or I/O resources. The stress levels used in this testing are considered to be at the top of the range of a typical user's needs.

TEST RESULTS

Test Scenario 1: Single Core EBX-38EAP - Passive and Active Performance

The figure below shows the thermal performance of the EBX-38EAP using the Atom E3815 processor.

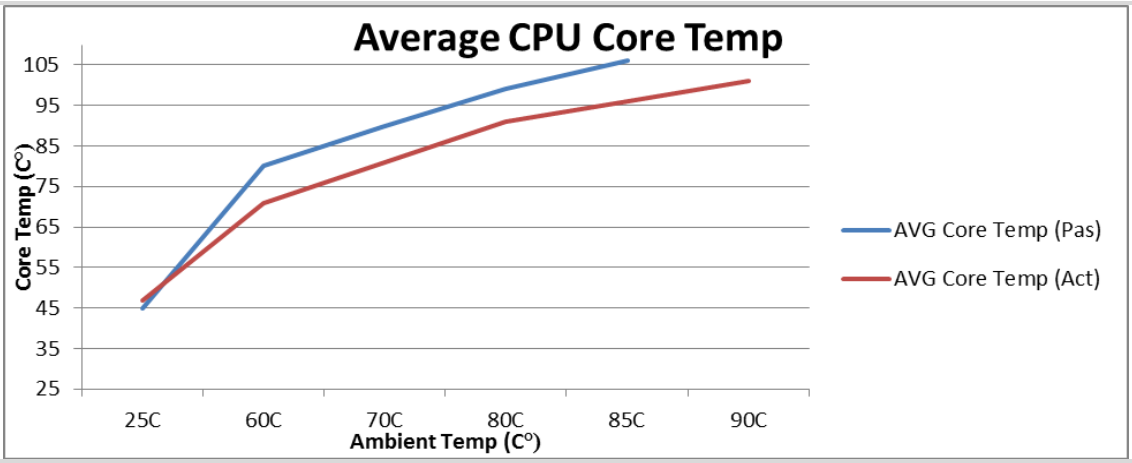
Figure 29. EBX-38EAP CPU Core Temperature Relative to Ambient Temperature



Test Scenario 2: Dual Core EBX-38EBP - Passive and Active Performance

This figure shows the thermal performance of the EBX-38EBP using the Atom E3826 processor.

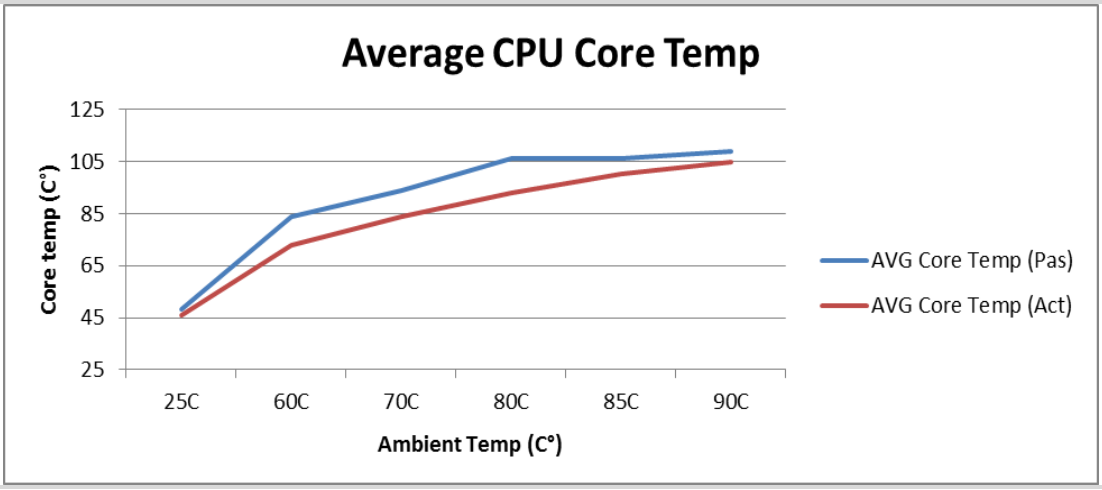
Figure 30. EBX-38EBP CPU Core Temperature Relative to Ambient Temperature



Test Scenario 3: Quad Core EBX-38ECP - Passive and Active Performance

The active and passive performance of the Atom E3845 version of the Viper will typically require a heat sink + fan for operation above 80 ºC, at >90% CPU utilization.

Figure 31. EBX-38ECP CPU Core Temperature Relative to Ambient Temperature



Installing the VersaLogic Thermal Solutions

The following thermal solution accessories are available from VersaLogic:

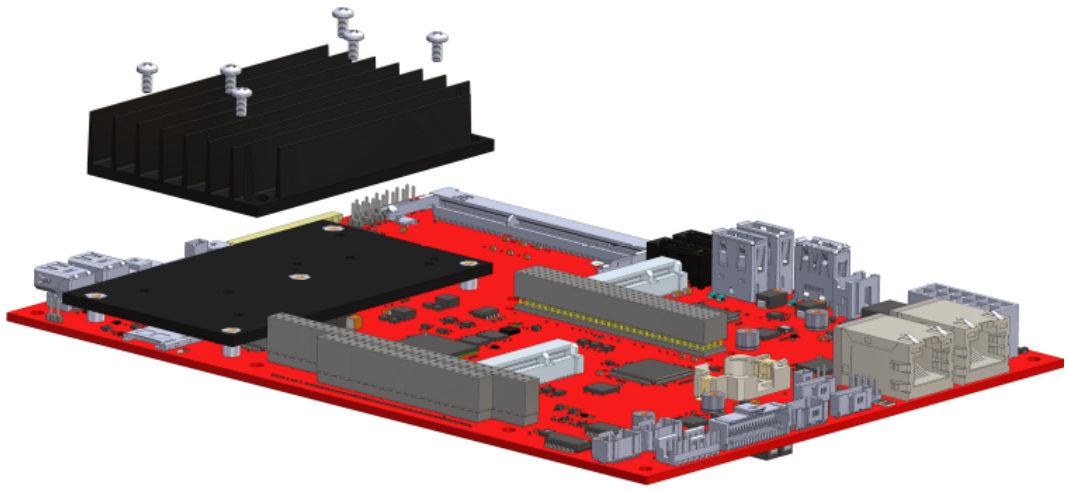
- VL-HDW-401 Thermal Compound Paste - used to mount the heat sink to the heat plate
- VL-HDW-406 Passive Heat Sink – mounts to standard product.
- VL-HDW-407 Fan Assembly – mounts to HDW-406 Heat Sink.

INSTALLING THE PASSIVE HEAT SINK

Install the passive heat sink (VL-HDW-406) using these steps:

1. **Apply the Arctic Silver† Thermal Compound**
   - Apply the thermal compound to the heat plate using the method described on the Arctic Silver website - http://www.arcticsilver.com/
2. **Position the passive heat sink**
   - Using the figure below as a guide, align the six mounting holes of the heat sink with the heat plate.
3. **Secure the passive heat sink to the heat plate**
   - Affix the passive heat sink to the heat plate using six M2.5 pan head screws.
   - Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.

Figure 32. Installing the Passive Heat Sink



INSTALLING THE HEAT SINK FAN

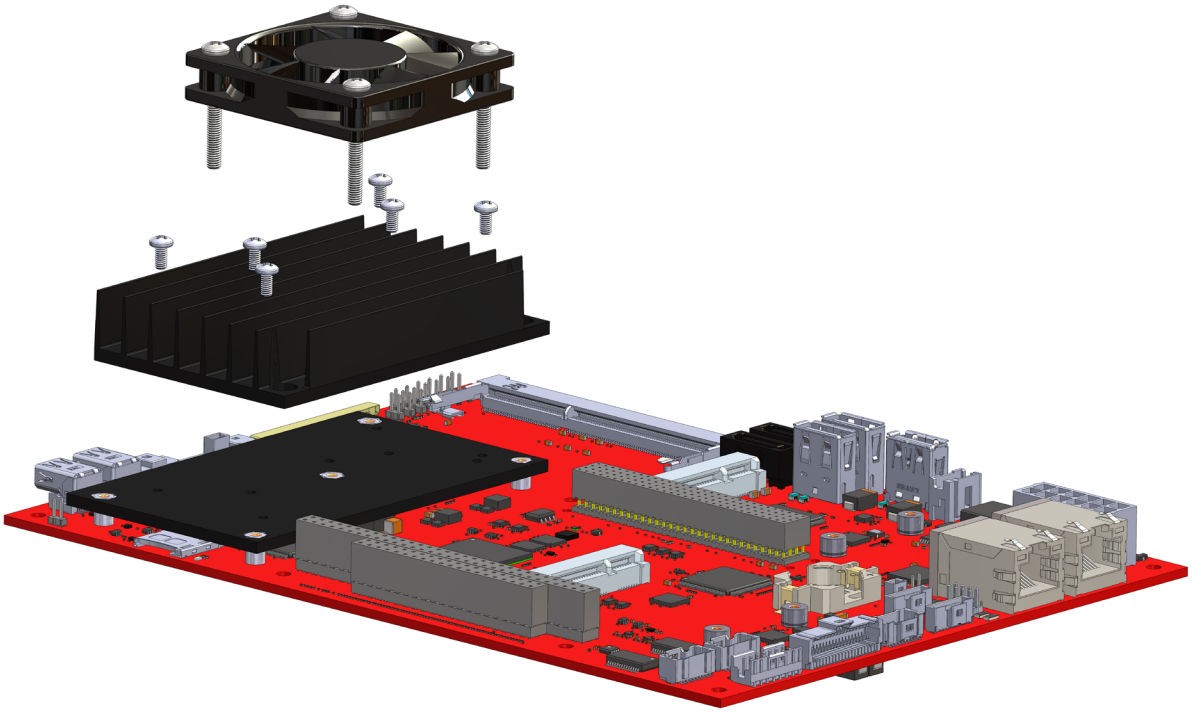
Install the heat sink fan (VL-HDW-407) using these steps:

1. **Position the fan assembly**

- Using the figure below as a guide, align the mounting holes of the heat sink fan with the four holes in the passive heat sink. Position the fan so that its power cable is on the side nearest the J24 CPU fan connector. The CPU fan connector is located between the Mini DisplayPort connector and the microSD socket (see Figure 2 on page 2).

2. **Secure the fan to the heat sink**
   - Affix the heat sink fan using four M3 pan head screws.
   - Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.
3. **Connect power to the fan**
   - Connect the fan's power cable to the J24 CPU fan connector on the Viper board.

Figure 33. Installing the Heat Sink Fan



- When the V9 jumper is not installed to enable the LVDS output, the LVDS resolution set by jumpers V6 and V7 will also select the VGA or DP resolution whenever the Screen Resolution is set as "Duplicate these displays" in Windows 7 Control Panel\All Control Panel Items\Display\Screen Resolution. If "Extend these displays" is selected, then the VGA or DP output may be set to a different resolution.
- The EBX-38EAP and EBX-38EBP SKUs are currently not speed stepping or throttling the CPU speed when the device gets hot.
- When the xHCI USB Host is enabled (enabling the USB 3.0 super speed), booting from a DOS USB thumb drive will not work. When necessary to boot DOS from a USB thumb drive, make sure the BIOS Setup selects the EHCI Host Controller instead.

*** *End of document* ***