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# FSBS5CH60

## Motion SPM® 3 Series

### Features

- UL Certified No. E209204 (UL1557)
- 600 V - 5 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low-Loss, Short-Circuit Rated IGBTs
- Low Thermal Resistance Using Ceramic Substrate
- Dedicated Vs Pins Simplify PCB Layout
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Isolation Rating: 2500 V<sub>rms</sub> / min.

### Applications

- Motion Control - Home Appliance / Industrial Motor

### Related Resources

- [AN-9035 - Motion SPM 3 Series Ver.2 User's Guide](#)

### General Description

FSBS5CH60 is a Motion SPM® 3 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

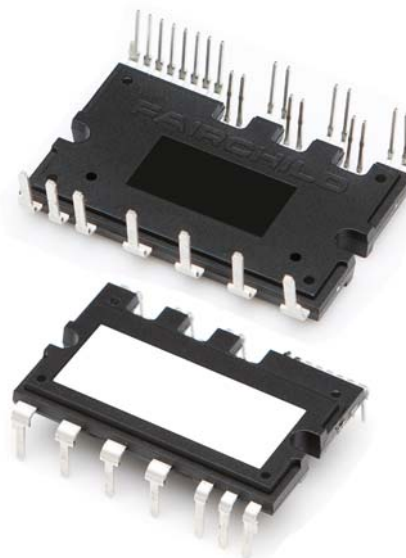


Figure 1. Package Overview

### Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FSBS5CH60	FSBS5CH60	SPMBA-027	Rail	10

### Integrated Power Functions

- 600 V - 5 A IGBT inverter for three-phase DC / AC power conversion (please refer to Figure 3)

### Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out Protection (UVLO)  
 Note: Available bootstrap circuit example is given in Figures 10 and 11.
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit Under-Voltage Lock-Out Protection (UVLO)
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3 / 5 V logic, Schmitt-trigger input

### Pin Configuration

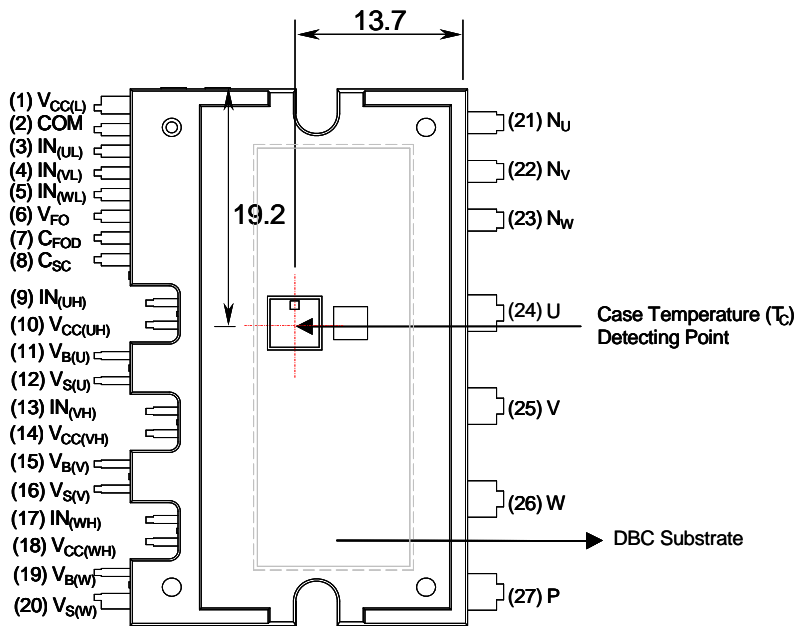


Figure 2. Top View

## Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-Side U-Phase
4	$IN_{(VL)}$	Signal Input for Low-Side V-Phase
5	$IN_{(WL)}$	Signal Input for Low-Side W-Phase
6	$V_{FO}$	Fault Output
7	$C_{FOD}$	Capacitor for Fault Output Duration Selection
8	$C_{SC}$	Capacitor (Low-pass Filter) for Short-Circuit Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-Side U-Phase
10	$V_{CC(UH)}$	High-Side Bias Voltage for U-Phase IC
11	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving
12	$V_{S(U)}$	High-Side Bias Voltage Ground for U-Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-Side V-Phase
14	$V_{CC(VH)}$	High-Side Bias Voltage for V-Phase IC
15	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
16	$V_{S(V)}$	High-Side Bias Voltage Ground for V-Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-Side W Phase
18	$V_{CC(WH)}$	High-Side Bias Voltage for W-Phase IC
19	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
20	$V_{S(W)}$	High-Side Bias Voltage Ground for W-Phase IGBT Driving
21	$N_U$	Negative DC-Link Input for U-Phase
22	$N_V$	Negative DC-Link Input for V-Phase
23	$N_W$	Negative DC-Link Input for W-Phase
24	U	Output for U-Phase
25	V	Output for V-Phase
26	W	Output for W-Phase
27	P	Positive DC-Link Input

### Internal Equivalent Circuit and Input/Output Pins



**Figure 3. Internal Block Diagram**

**1st Notes:**

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

## Absolute Maximum Ratings ( $T_J = 25^\circ\text{C}$ , unless otherwise specified.)

### Inverter Part

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN}$	Supply Voltage	Applied between P- $N_U$ , $N_V$ , $N_W$	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P- $N_U$ , $N_V$ , $N_W$	500	V
$V_{CES}$	Collector - Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$	5	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$ , Under 1ms Pulse Width	10	A
$P_C$	Collector Dissipation	$T_C = 25^\circ\text{C}$ per Chip	25	W
$T_J$	Operating Junction Temperature	(2nd Note 1)	-20 ~ 125	$^\circ\text{C}$

#### 2nd Notes:

- The maximum junction temperature rating of the power chips integrated within the Motion SPM® 3 product is  $150^\circ\text{C}$  (at  $T_C \leq 100^\circ\text{C}$ ). However, to insure safe operation of the Motion SPM 3 product, the average junction temperature should be limited to  $T_{J(\text{ave})} \leq 125^\circ\text{C}$  (at  $T_C \leq 100^\circ\text{C}$ )

### Control Part

Symbol	Parameter	Conditions	Rating	Unit
$V_{CC}$	Control Supply Voltage	Applied between $V_{CC(\text{UH})}$ , $V_{CC(\text{VH})}$ , $V_{CC(\text{WH})}$ , $V_{CC(\text{L})}$ - COM	20	V
$V_{BS}$	High-Side Control Bias Voltage	Applied between $V_{B(\text{U})} - V_{S(\text{U})}$ , $V_{B(\text{V})} - V_{S(\text{V})}$ , $V_{B(\text{W})} - V_{S(\text{W})}$	20	V
$V_{IN}$	Input Signal Voltage	Applied between $IN_{(\text{UH})}$ , $IN_{(\text{VH})}$ , $IN_{(\text{WH})}$ , $IN_{(\text{UL})}$ , $IN_{(\text{VL})}$ , $IN_{(\text{WL})}$ - COM	-0.3 ~ 17	V
$V_{FO}$	Fault Output Supply Voltage	Applied between $V_{FO}$ - COM	-0.3 ~ $V_{CC}+0.3$	V
$I_{FO}$	Fault Output Current	Sink Current at $V_{FO}$ Pin	5	mA
$V_{SC}$	Current-Sensing Input Voltage	Applied between $C_{SC}$ - COM	-0.3 ~ $V_{CC}+0.3$	V

### Total System

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(\text{PROT})}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}$ $T_J = 125^\circ\text{C}$ , Non-Repetitive, $< 2 \mu\text{s}$	400	V
$T_C$	Module Case Operation Temperature	$-20^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$ , See Figure 2	-20 ~ 100	$^\circ\text{C}$
$T_{STG}$	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage	60 Hz, Sinusoidal, AC 1 Minute, Connect Pins to Heat Sink Plate	2500	$V_{\text{rms}}$

### Thermal Resistance

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT Part (per 1 / 6 module)	-	-	3.9	$^\circ\text{C/W}$
$R_{th(j-c)F}$		Inverter FWD Part (per 1 / 6 module)	-	-	5.3	$^\circ\text{C/W}$

#### 2nd Notes:

- For the measurement point of case temperature( $T_C$ ), please refer to Figure 2.



## Electrical Characteristics (T<sub>J</sub> = 25°C, unless otherwise specified.)

### Control Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I <sub>QCCL</sub>	Quiescent V <sub>CC</sub> Supply Current	V <sub>CC</sub> = 15 V I <sub>N(U<sub>L</sub>, V<sub>L</sub>, W<sub>L</sub>)</sub> = 0 V	V <sub>CC(L)</sub> - COM	-	-	23	mA
I <sub>QCCH</sub>		V <sub>CC</sub> = 15 V I <sub>N(U<sub>H</sub>, V<sub>H</sub>, W<sub>H</sub>)</sub> = 0 V	V <sub>CC(U<sub>H</sub>)</sub> , V <sub>CC(V<sub>H</sub>)</sub> , V <sub>CC(W<sub>H</sub>)</sub> - COM	-	-	100	μA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>BS</sub> = 15 V I <sub>N(U<sub>H</sub>, V<sub>H</sub>, W<sub>H</sub>)</sub> = 0 V	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	-	500	μA
V <sub>FOH</sub>	Fault Output Voltage	V <sub>SC</sub> = 0 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up	4.5	-	-	V	
V <sub>FOL</sub>		V <sub>SC</sub> = 1 V, V <sub>FO</sub> Circuit: 4.7 kΩ to 5 V Pull-up	-	-	0.8	V	
V <sub>SC(ref)</sub>	Short Circuit Current Trip Level	V <sub>CC</sub> = 15 V (2nd Note 4)	0.45	0.50	0.55	V	
UV <sub>CCD</sub>	Supply Circuit Under-Voltage Protection	Detection Level	10.7	11.9	13.0	V	
UV <sub>CCR</sub>		Reset Level	11.2	12.4	13.2	V	
UV <sub>BSD</sub>		Detection Level	10.1	11.3	12.5	V	
UV <sub>BSR</sub>		Reset Level	10.5	11.7	12.9	V	
t <sub>FOD</sub>	Fault-out Pulse Width	C <sub>FOD</sub> = 33 nF (2nd Note 5)	1.0	1.8	-	ms	
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between I <sub>N(U<sub>H</sub>)</sub> , I <sub>N(V<sub>H</sub>)</sub> , I <sub>N(W<sub>H</sub>)</sub> , I <sub>N(U<sub>L</sub>)</sub> , I <sub>N(V<sub>L</sub>)</sub> , I <sub>N(W<sub>L</sub>)</sub> - COM	3.0	-	-	V	
V <sub>IN(OFF)</sub>	OFF Threshold Voltage		-	-	0.8	V	

#### 2nd Notes:

4. Short-circuit protection is functioning only at the low-sides.

5. The fault-out pulse width t<sub>FOD</sub> depends on the capacitance value of C<sub>FOD</sub> according to the following approximate equation: C<sub>FOD</sub> = 18.3 × 10<sup>-6</sup> × t<sub>FOD</sub> [F]

### Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>PN</sub>	Supply Voltage	Applied between P - N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub>	-	300	400	V
V <sub>CC</sub>	Control Supply Voltage	Applied between V <sub>CC(U<sub>H</sub>)</sub> , V <sub>CC(V<sub>H</sub>)</sub> , V <sub>CC(W<sub>H</sub>)</sub> , V <sub>CC(L)</sub> - COM	13.5	15	16.5	V
V <sub>BS</sub>	High-Side Bias Voltage	Applied between V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	13.0	15	18.5	V
dV <sub>CC</sub> / dt, dV <sub>BS</sub> / dt	Control Supply Variation		-1	-	1	V / μs
t <sub>dead</sub>	Blanking Time for Preventing Arm-Short	For Each Input Signal	2.0	-	-	μs
f <sub>PWM</sub>	PWM Input Signal	-20°C ≤ T <sub>C</sub> ≤ 100°C, -20°C ≤ T <sub>J</sub> ≤ 125°C	-	-	20	kHz
V <sub>SEN</sub>	Voltage for Current Sensing	Applied between N <sub>U</sub> , N <sub>V</sub> , N <sub>W</sub> - COM (Including Surge Voltage)	-4		4	V



### Mechanical Characteristics and Ratings

Parameter	Conditions		Min.	Typ.	Max.	Unit
Mounting Torque	Mounting Screw: M3	Recommended 0.62 N•m	0.51	0.62	0.72	N•m
Device Flatness		See Figure 5	0	-	+120	μm
Weight			-	15.40	-	g



**Figure 5. Flatness Measurement Position**

### Time Charts of Protective Function



- a1 : Control supply voltage rises: after the voltage rises  $UV_{CCR}$ , the circuits start to operate when next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under-Voltage detection ( $UV_{CCD}$ ).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts.
- a6 : Under-Voltage reset ( $UV_{CCR}$ ).
- a7 : Normal operation: IGBT ON and carrying current.

**Figure 6. Under-Voltage Protection (Low-Side)**



- b1 : Control supply voltage rises: after the voltage reaches  $UV_{BSR}$ , the circuits start to operate when next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under-Voltage detection ( $UV_{BSD}$ ).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under-Voltage reset ( $UV_{BSR}$ ).
- b6 : Normal operation: IGBT ON and carrying current.

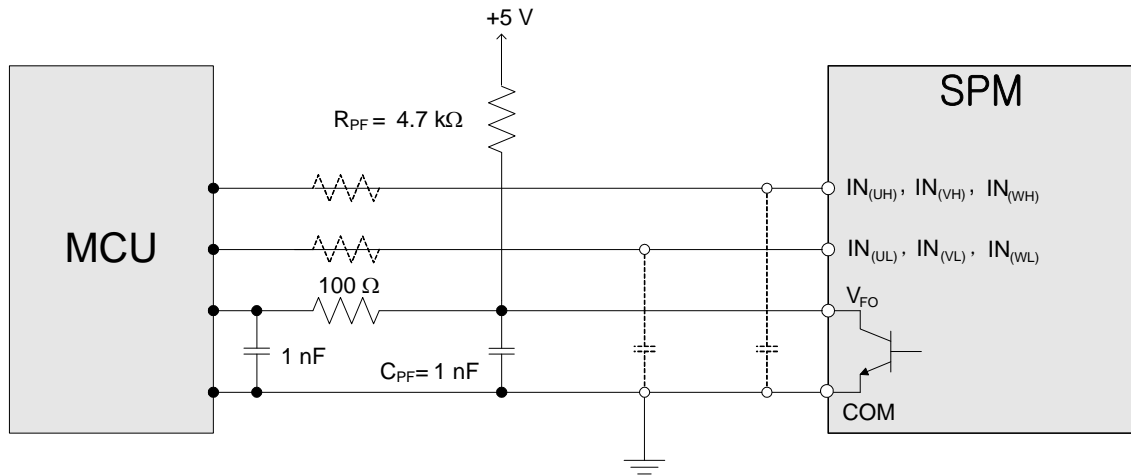
**Figure 7. Under-Voltage Protection (High-Side)**



(with the external shunt resistance and CR connection)

- c1 : Normal operation: IGBT ON and carrying current.
- c2 : Short-Circuit current detection (SC trigger).
- c3 : Hard IGBT gate interrupt.
- c4 : IGBT turns OFF.
- c5 : Fault output timer operation starts: the pulse width of the fault output signal is set by the external capacitor  $C_{FO}$ .
- c6 : Input "LOW": IGBT OFF state.
- c7 : Input "HIGH": IGBT ON state, but during the active period of fault output, the IGBT doesn't turn ON.
- c8 : IGBT OFF state.

**Figure 8. Short-Circuit Protection (Low-Side Operation Only)**



**Figure 9. Recommended MCU I/O Interface Circuit**

**3rd Notes:**

1. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The Motion SPM® 3 Product input signal section integrates a 3.3 kΩ(typ.) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the signal voltage drop at input terminal.
2. The logic input works with standard CMOS or LSTTL outputs.



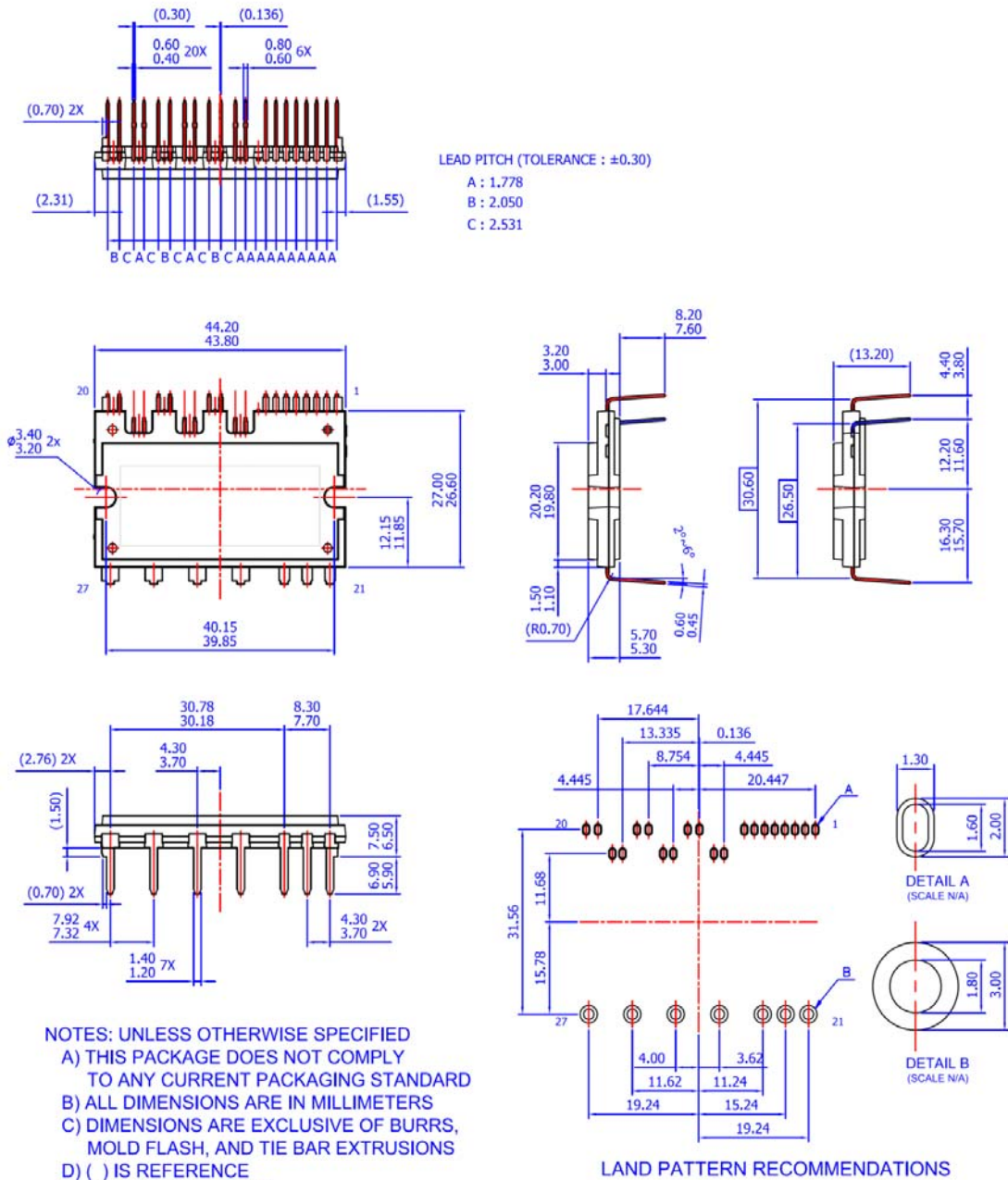
**Figure 10. Recommended Bootstrap Operation Circuit and Parameters**

**3rd Notes:**

3. It would be recommended that the bootstrap diode,  $D_{BS}$ , has soft and fast recovery characteristics.
4. The bootstrap resistor ( $R_{BS}$ ) should be three times greater than  $R_{E(H)}$ . The recommended value of  $R_{E(H)}$  is 5.6 Ω, but it can be increased up to 20 Ω (maximum) for a slower  $dv/dt$  of high-side.
5. The ceramic capacitor placed between  $V_{CC}$  - COM should be over 1 μF and mounted as close to the pins of the Motion SPM 3 product as possible.



## Detailed Package Outline Drawings



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