74HC40103

8-bit synchronous binary down counter

Rev. 4 — 27 January 2016 Product data sheet

1. General description

The 74HC40103 is an 8-bit synchronous down counter. It has control inputs for enabling or disabling the clock (CP), for clearing the counter to its maximum count and for presetting the counter either synchronously or asynchronously. In normal operation, the counter is decremented by one count on each positive-going transition of the clock (CP). Counting is inhibited when the terminal enable input ($\overline{TE}$) is HIGH. The terminal count output ($\overline{TC}$) goes LOW when the count reaches zero if $\overline{TE}$ is LOW, and remains LOW for one full clock period. When the synchronous preset enable input ($\overline{PE}$) is LOW, data at the jam input (P0 to P7) is clocked into the counter on the next positive-going clock transition regardless of the state of $\overline{TE}$. When the asynchronous preset enable input ($\overline{PL}$) is LOW, data at the jam input (P0 to P7) is asynchronously forced into the counter regardless of the state of $\overline{PE}$, $\overline{TE}$, or CP. The jam inputs (P0 to P7) represent a single 8-bit binary word. When the master reset input ($\overline{MR}$) is LOW, the counter is asynchronously cleared to its maximum count (decimal 255) regardless of the state of any other input. If all control inputs except $\overline{TE}$ are HIGH at the time of zero count, the counters will jump to the maximum count, giving a counting sequence of 256 clock pulses long. Device may be cascaded using the $\overline{TE}$ input and the TC output, in either a synchronous or ripple mode. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Cascadable
- Synchronous or asynchronous preset
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- Input levels:
  - For 74HC40103: CMOS level
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C

3. Applications

- Divide-by-n counters
- Programmable timers
- Interrupt timers

- Cycle/program counters.

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC40103D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC40103DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC40103PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

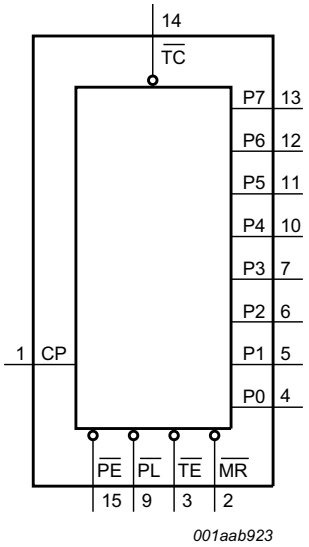


Fig 1. Functional diagram

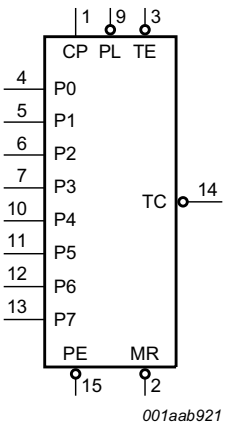


Fig 2. Logic symbol

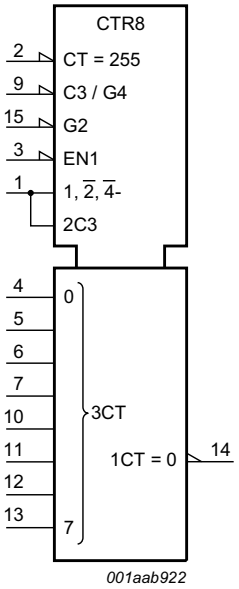


Fig 3. IEC logic symbol

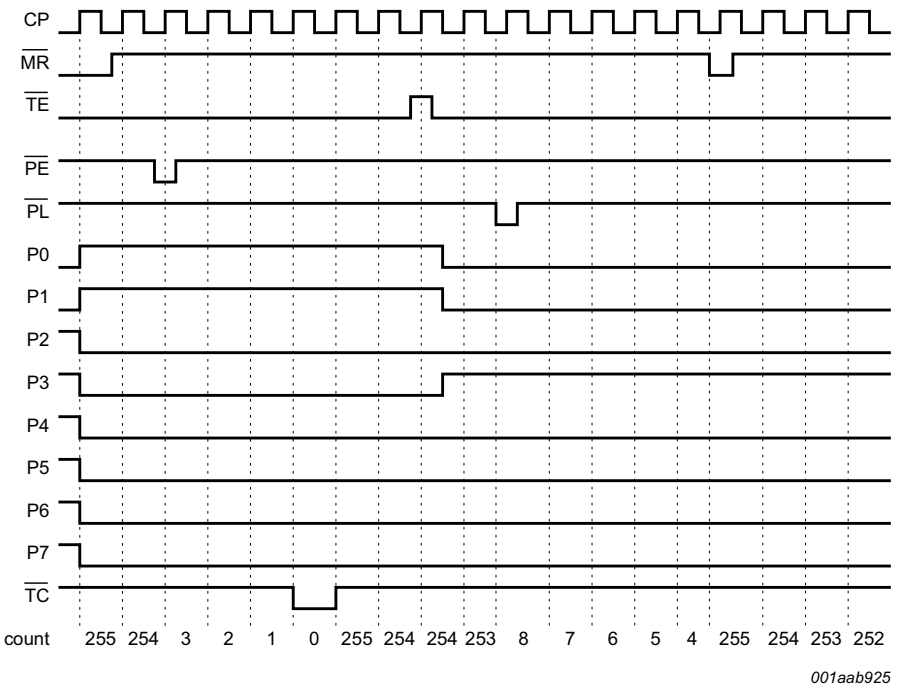


Fig 4. Timing diagram

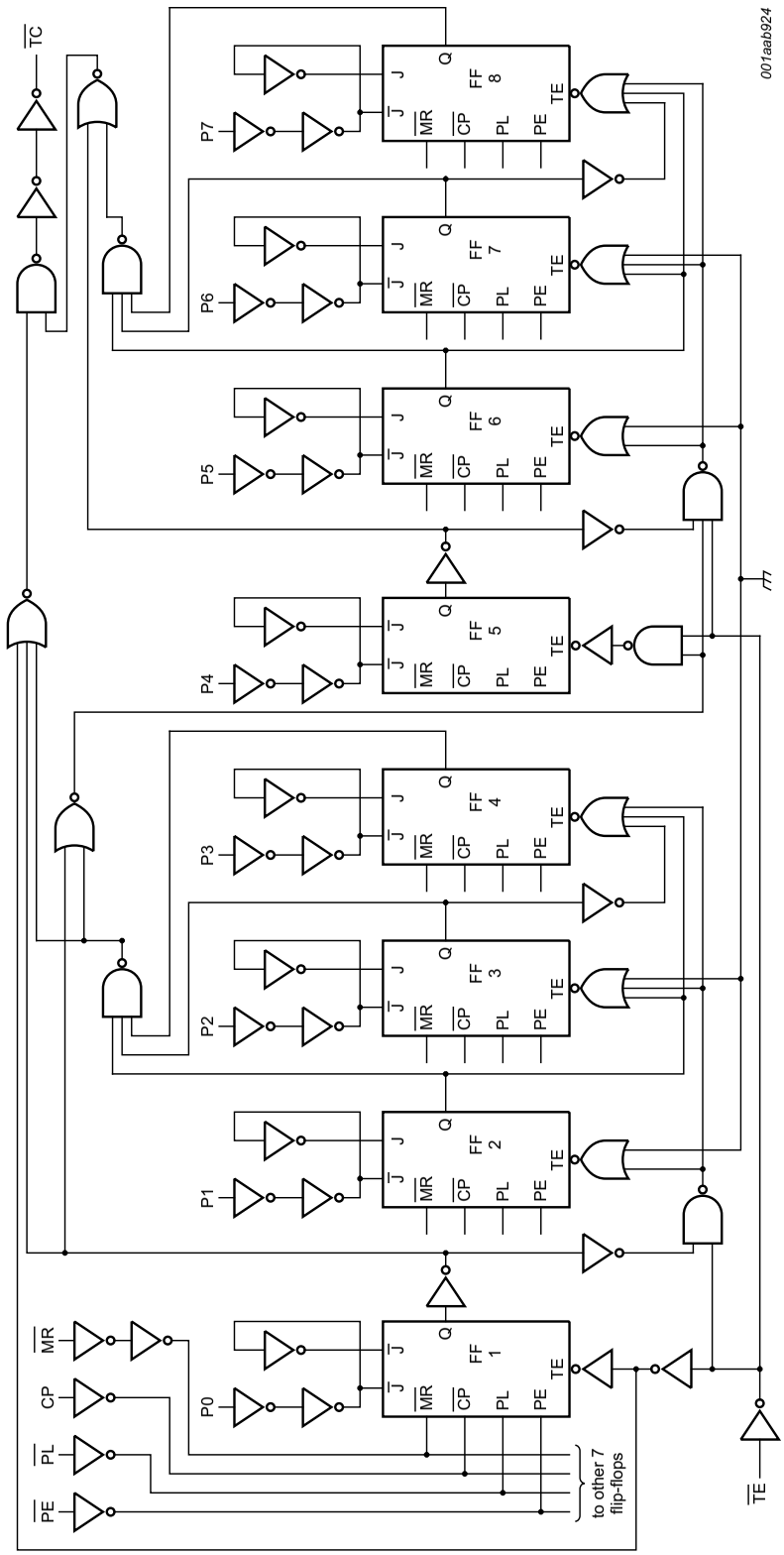


Fig 5. Logic diagram

6. Pinning information

6.1 Pinning

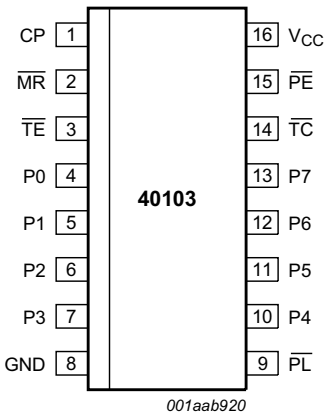


Fig 6. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CP	1	clock input (LOW-to-HIGH, edge-triggered)
$\overline{MR}$	2	asynchronous master reset input (active LOW)
$\overline{TE}$	3	terminal enable input (active LOW)
P0	4	jam input 0
P1	5	jam input 1
P2	6	jam input 2
P3	7	jam input 3
GND	8	ground (0 V)
$\overline{PL}$	9	asynchronous preset enable input (active LOW)
P4	10	jam input 4
P5	11	jam input 5
P5	12	jam input 6
P7	13	jam input 7
$\overline{TC}$	14	terminal count output (active LOW)
$\overline{PE}$	15	synchronous preset enable input (active LOW)
V_{CC}	16	positive supply voltage

7. Functional description

7.1 Function table

Table 3. Function table[1]

Control inputs				Preset mode	Action[2]
$\overline{MR}$	$\overline{PL}$	$\overline{PE}$	$\overline{TE}$		
L	X	X	X	asynchronous	clear to maximum count
H	L	X	X	asynchronous	preset asynchronously
	H	L	X	synchronous	preset on next LOW-to HIGH clock transition
		H	L	synchronous	count down
			H	synchronous	inhibit counter

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

[2] Clock connected to CP.
Synchronous operation: changes occur on the LOW-to-HIGH CP transition.
Jam inputs: MSD = P7, LSD = P0.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	+50	mA
I_{GND}	ground current			−50	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	SO16 package	[2]	-	500	mW
		SSOP16 and TSSOP16 packages	[3]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C, P_{tot} derates linearly with 8 mW/K.

[3] For SSOP16 and TSSOP16 packages: above 60 °C, P_{tot} derates linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rates	V_{CC} = 2.0 V	-	-	625	ns
		V_{CC} = 4.5 V	-	1.67	139	ns
		V_{CC} = 6.0 V	-	-	83	ns
T_{amb}	ambient temperature		−40	-	+125	°C

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	μA
C_I	input capacitance		-	3.5	-	pF

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	μA
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = –4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	μA

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{pd}	propagation delay	CP to $\overline{TC}$; see Figure 7 [1]				
		V_{CC} = 2.0 V	-	96	300	ns
		V_{CC} = 4.5 V	-	35	60	ns
		V_{CC} = 6.0 V	-	28	51	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	30	-	ns
		$\overline{TE}$ to $\overline{TC}$; see Figure 8				
		V_{CC} = 2.0 V	-	50	175	ns
		V_{CC} = 4.5 V	-	18	35	ns
		V_{CC} = 6.0 V	-	14	30	ns
		$\overline{PL}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	102	315	ns
		V_{CC} = 4.5 V	-	37	63	ns
		V_{CC} = 6.0 V	-	30	53	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	83	275	ns
		V_{CC} = 4.5 V	-	30	55	ns
		V_{CC} = 6.0 V	-	24	47	ns
t_t	transition time	see Figure 8 [2]				
		V_{CC} = 2.0 V	-	19	75	ns
		V_{CC} = 4.5 V	-	7	15	ns
		V_{CC} = 6.0 V	-	6	13	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	pulse width	CP HIGH or LOW; see Figure 7				
		V_{CC} = 2.0 V	165	22	-	ns
		V_{CC} = 4.5 V	33	8	-	ns
		V_{CC} = 6.0 V	28	6	-	ns
		$\overline{MR}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	125	39	-	ns
		V_{CC} = 4.5 V	25	14	-	ns
		V_{CC} = 6.0 V	21	11	-	ns
		$\overline{PL}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	125	33	-	ns
		V_{CC} = 4.5 V	25	12	-	ns
		V_{CC} = 6.0 V	21	10	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP, $\overline{PL}$ to CP; see Figure 10				
		V_{CC} = 2.0 V	50	14	-	ns
		V_{CC} = 4.5 V	10	5	-	ns
		V_{CC} = 6.0 V	9	4	-	ns
t_{su}	set-up time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	75	22	-	ns
		V_{CC} = 4.5 V	15	8	-	ns
		V_{CC} = 6.0 V	13	6	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	150	44	-	ns
		V_{CC} = 4.5 V	30	16	-	ns
		V_{CC} = 6.0 V	26	13	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	75	22	-	ns
		V_{CC} = 4.5 V	15	8	-	ns
		V_{CC} = 6.0 V	13	6	-	ns
t_h	hold time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	0	–14	-	ns
		V_{CC} = 4.5 V	0	–5	-	ns
		V_{CC} = 6.0 V	0	–4	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	0	–30	-	ns
		V_{CC} = 4.5 V	0	–11	-	ns
		V_{CC} = 6.0 V	0	–9	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	0	–17	-	ns
		V_{CC} = 4.5 V	0	–6	-	ns
		V_{CC} = 6.0 V	0	–5	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum frequency	see Figure 7				
		V_{CC} = 2.0 V	3.0	10	-	MHz
		V_{CC} = 4.5 V	15	29	-	MHz
		V_{CC} = 6.0 V	18	35	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	32	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [3]	-	24	-	pF
T_{amb} = –40 °C to +85 °C						
t_{pd}	propagation delay	CP to $\overline{TC}$; see Figure 7 [1]				
		V_{CC} = 2.0 V	-	-	375	ns
		V_{CC} = 4.5 V	-	-	75	ns
		V_{CC} = 6.0 V	-	-	64	ns
		$\overline{TE}$ to $\overline{TC}$; see Figure 8				
		V_{CC} = 2.0 V	-	-	220	ns
		V_{CC} = 4.5 V	-	-	44	ns
		V_{CC} = 6.0 V	-	-	37	ns
		$\overline{PL}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	-	395	ns
		V_{CC} = 4.5 V	-	-	79	ns
		V_{CC} = 6.0 V	-	-	40	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	-	345	ns
		V_{CC} = 4.5 V	-	-	69	ns
		V_{CC} = 6.0 V	-	-	59	ns
t_t	transition time	see Figure 8 [2]				
		V_{CC} = 2.0 V	-	-	95	ns
		V_{CC} = 4.5 V	-	-	19	ns
		V_{CC} = 6.0 V	-	-	16	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7				
		V_{CC} = 2.0 V	205	-	-	ns
		V_{CC} = 4.5 V	41	-	-	ns
		V_{CC} = 6.0 V	35	-	-	ns
		$\overline{MR}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	155	-	-	ns
		V_{CC} = 4.5 V	31	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns
		$\overline{PL}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	155	-	-	ns
		V_{CC} = 4.5 V	31	-	-	ns
		V_{CC} = 6.0 V	26	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rec}	recovery time	$\overline{MR}$ to CP, $\overline{PL}$ to CP; see Figure 10				
		V_{CC} = 2.0 V	65	-	-	ns
		V_{CC} = 4.5 V	13	-	-	ns
		V_{CC} = 6.0 V	11	-	-	ns
t_{su}	set-up time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	33	-	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	95	-	-	ns
		V_{CC} = 4.5 V	19	-	-	ns
		V_{CC} = 6.0 V	16	-	-	ns
t_h	hold time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
f_{max}	maximum frequency	see Figure 7				
		V_{CC} = 2.0 V	2.4	-	-	MHz
		V_{CC} = 4.5 V	12	-	-	MHz
		V_{CC} = 6.0 V	14	-	-	MHz

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +125 °C						
t_{pd}	propagation delay	CP to $\overline{TC}$; see Figure 7 [1]				
		V_{CC} = 2.0 V	-	-	450	ns
		V_{CC} = 4.5 V	-	-	90	ns
		V_{CC} = 6.0 V	-	-	77	ns
		$\overline{TE}$ to $\overline{TC}$; see Figure 8				
		V_{CC} = 2.0 V	-	-	265	ns
		V_{CC} = 4.5 V	-	-	53	ns
		V_{CC} = 6.0 V	-	-	45	ns
		$\overline{PL}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	-	475	ns
		V_{CC} = 4.5 V	-	-	95	ns
		V_{CC} = 6.0 V	-	-	81	ns
t_{PHL}	HIGH to LOW propagation delay	$\overline{MR}$ to $\overline{TC}$; see Figure 9				
		V_{CC} = 2.0 V	-	-	415	ns
		V_{CC} = 4.5 V	-	-	83	ns
		V_{CC} = 6.0 V	-	-	71	ns
t_t	transition time	see Figure 8 [2]				
		V_{CC} = 2.0 V	-	-	110	ns
		V_{CC} = 4.5 V	-	-	22	ns
		V_{CC} = 6.0 V	-	-	19	ns
t_W	pulse width	CP HIGH or LOW; see Figure 7				
		V_{CC} = 2.0 V	250	-	-	ns
		V_{CC} = 4.5 V	50	-	-	ns
		V_{CC} = 6.0 V	43	-	-	ns
		$\overline{MR}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	32	-	-	ns
		$\overline{PL}$ LOW; see Figure 9				
		V_{CC} = 2.0 V	190	-	-	ns
		V_{CC} = 4.5 V	38	-	-	ns
		V_{CC} = 6.0 V	32	-	-	ns
t_{rec}	recovery time	$\overline{MR}$ to CP, $\overline{PL}$ to CP; see Figure 10				
		V_{CC} = 2.0 V	75	-	-	ns
		V_{CC} = 4.5 V	15	-	-	ns
		V_{CC} = 6.0 V	13	-	-	ns

Table 7. Dynamic characteristics *...continued*

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF; see Figure 13.

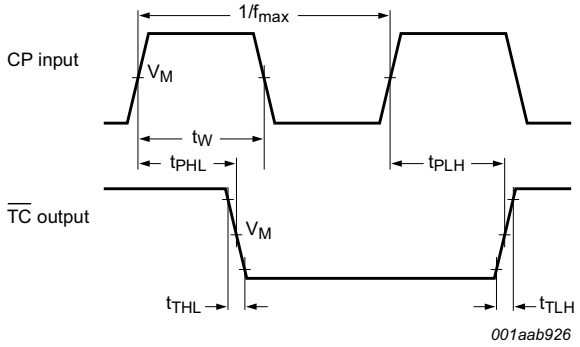
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	225	-	-	ns
		V_{CC} = 4.5 V	45	-	-	ns
		V_{CC} = 6.0 V	38	-	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	110	-	-	ns
		V_{CC} = 4.5 V	22	-	-	ns
		V_{CC} = 6.0 V	19	-	-	ns
t_h	hold time	$\overline{PE}$ to CP; see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
		$\overline{TE}$ to CP; see Figure 12				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
		Pn to CP; see Figure 11				
		V_{CC} = 2.0 V	0	-	-	ns
		V_{CC} = 4.5 V	0	-	-	ns
		V_{CC} = 6.0 V	0	-	-	ns
f_{max}	maximum frequency	see Figure 7				
		V_{CC} = 2.0 V	2.0	-	-	MHz
		V_{CC} = 4.5 V	10	-	-	MHz
		V_{CC} = 6.0 V	12	-	-	MHz

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

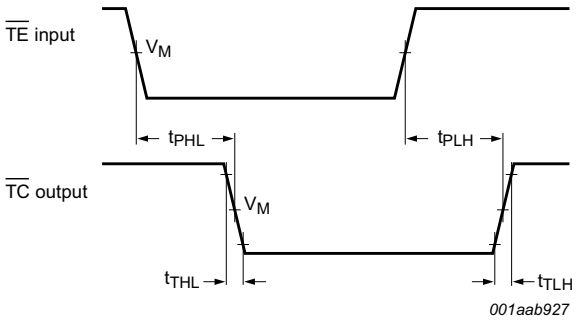
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

12. Waveforms



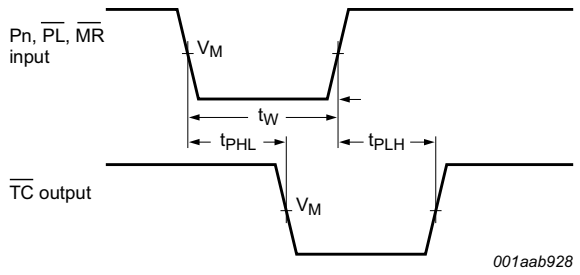
$V_M = 0.5 \times V_I$

Fig 7. Waveforms showing the clock input (CP) to TC propagation delays, the clock pulse width, the output transition times and the maximum clock pulse frequency



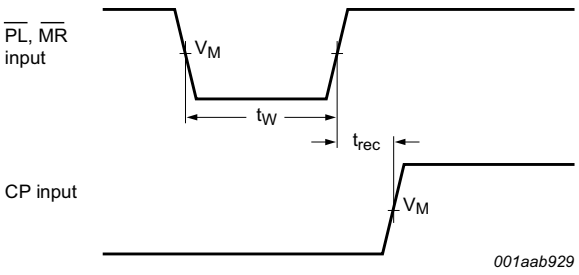
$V_M = 0.5 \times V_I$

Fig 8. Waveforms showing the $\overline{TE}$ to $\overline{TC}$ propagation delays



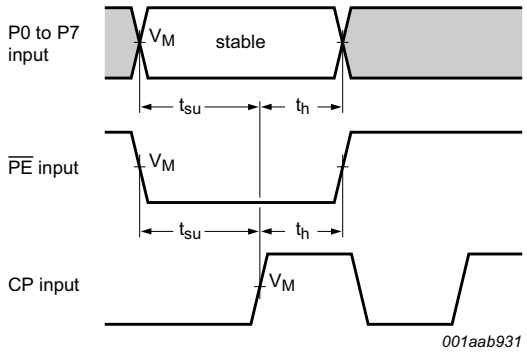
$V_M = 0.5 \times V_I$

Fig 9. Waveforms showing $\overline{PL}$, $\overline{MR}$, Pn to $\overline{TC}$ propagation delays



$V_M = 0.5 \times V_I$

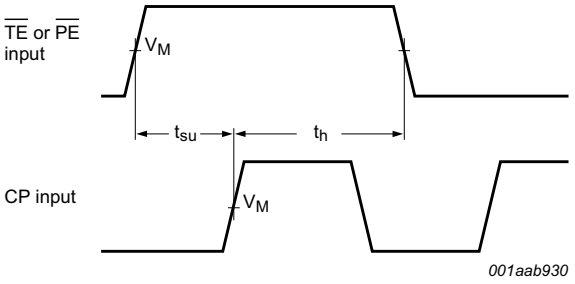
Fig 10. Waveforms showing removal time for $\overline{MR}$ and $\overline{PL}$



The shaded areas indicate when the input is permitted to change for predictable output performance.

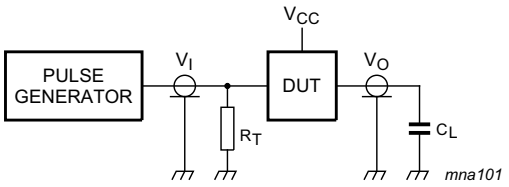
$V_M = 0.5 \times V_I$

Fig 11. Waveforms showing hold and set-up times for Pn, PE to CP



$V_M = 0.5 \times V_I$

Fig 12. Waveforms showing hold and set-up times for MR or PE to CP



Test data is given in Table 8.

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 13. Test circuit for measuring switching times

Table 8. Test data

Supply	Input		Load
V_{CC}	V_I	t_r, t_f	C_L
2.0 V	V_{CC}	6 ns	50 pF
4.5 V	V_{CC}	6 ns	50 pF
6.0 V	V_{CC}	6 ns	50 pF
5.0 V	V_{CC}	6 ns	15 pF

13. Application information

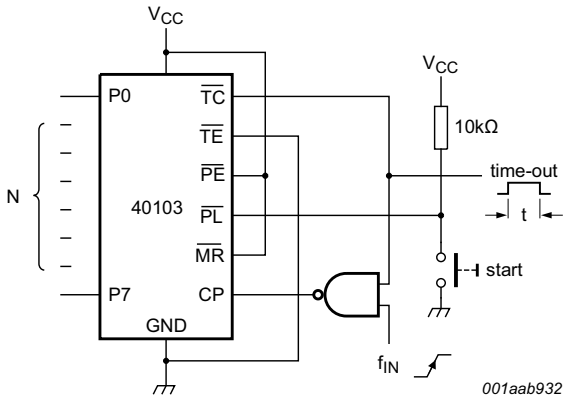


Fig 14. Programmable timer

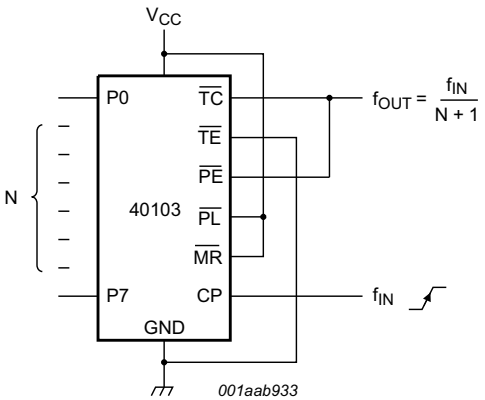
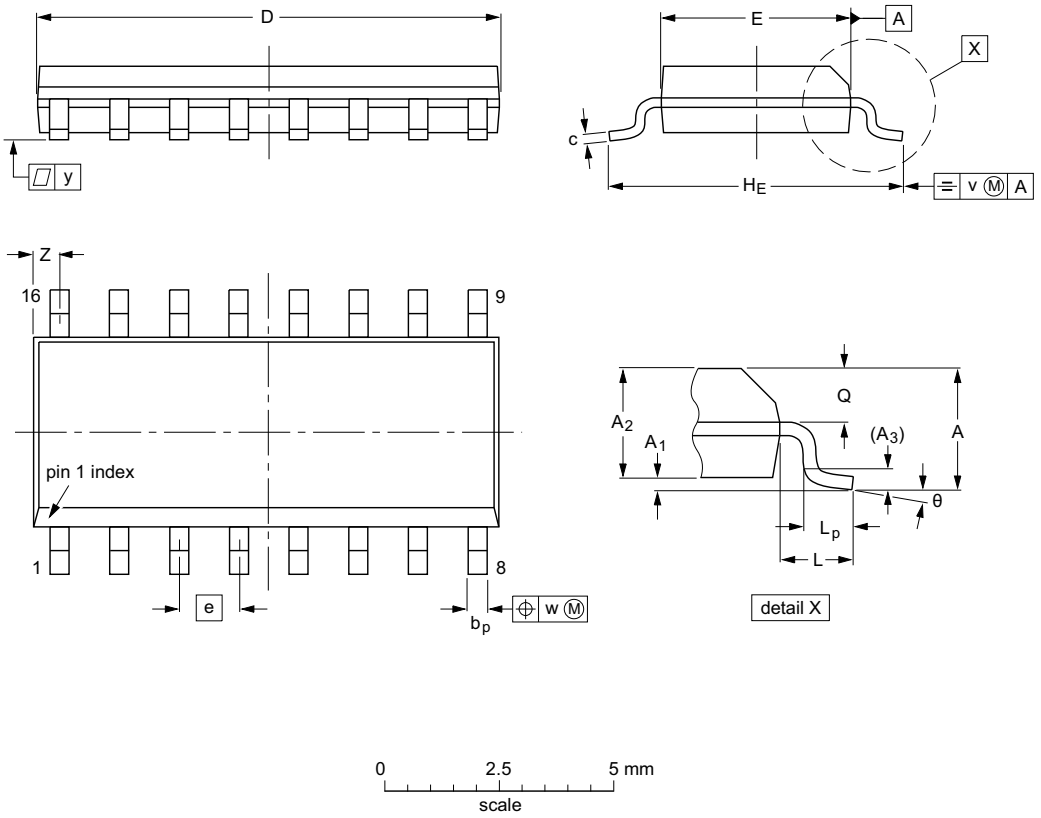


Fig 15. Divide-by-N counter

14. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

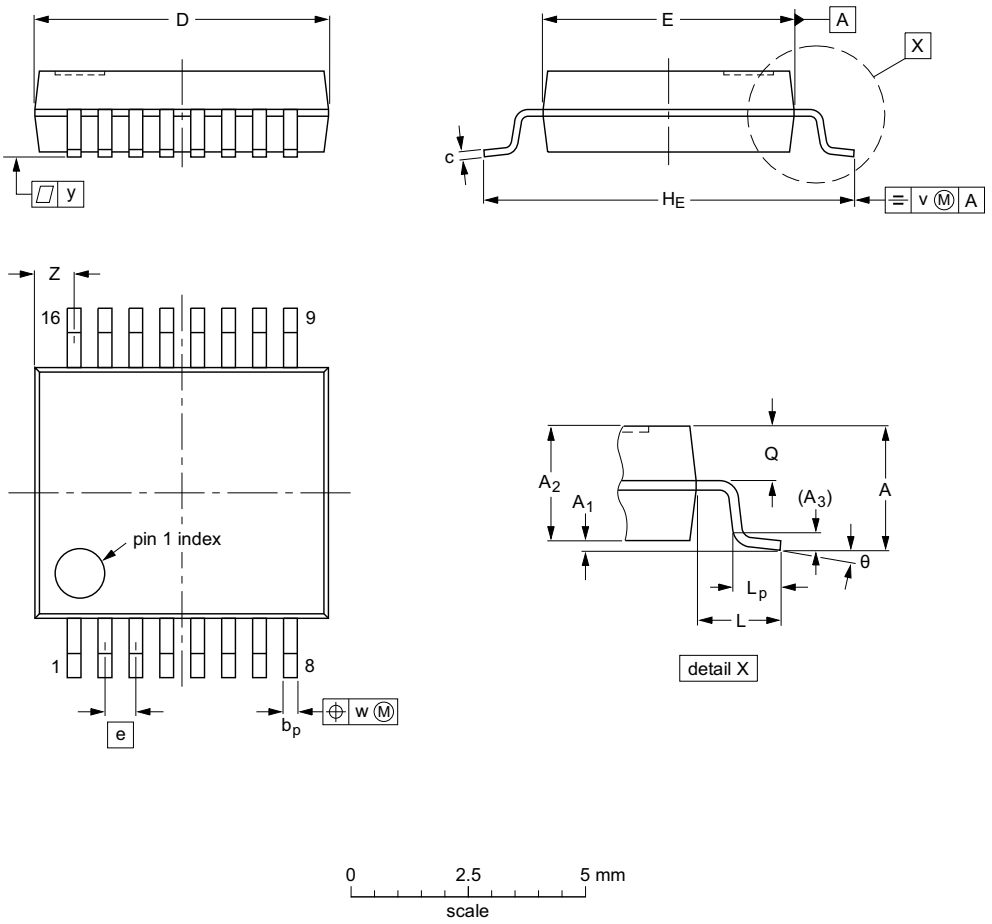
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

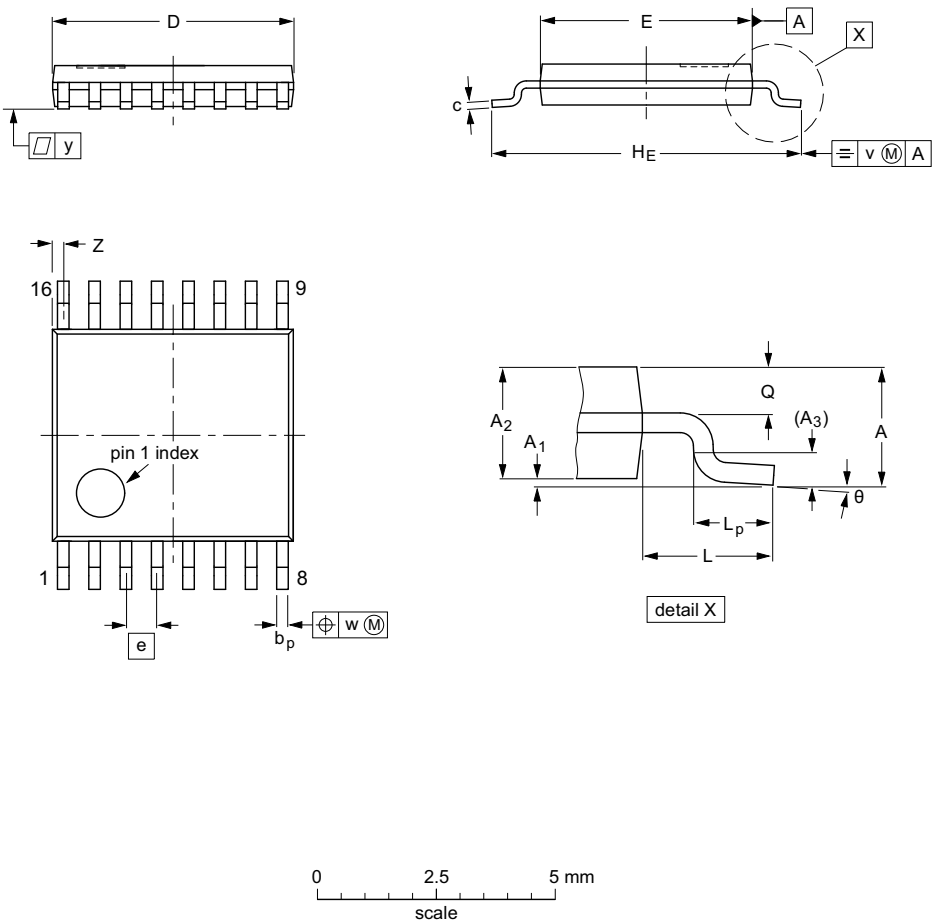
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 18. Package outline SOT403-1 (TSSOP16)

15. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

16. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC40103 v.4	20160127	Product data sheet	-	74HC40103 v.3
Modifications:	• Type number 74HC40103N (SOT38-4) removed.			
74HC40103 v.3	20041112	Product data sheet	-	74HC_HCT40103_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the current presentation and information standard of Philips Semiconductors. • Removed type number 74HCT40103. • Inserted family specification.			
74HC_HCT40103_CNV v.2	19970918	Product specification	-	74HC_HCT40103 v.1
74HC_HCT40103 v.1	19901201	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents

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Date of release: 27 January 2016
Document identifier: 74HC40103